COMPACT DISC PLAYER

KDC-80

SERVICE MANUAL

KENWOOD

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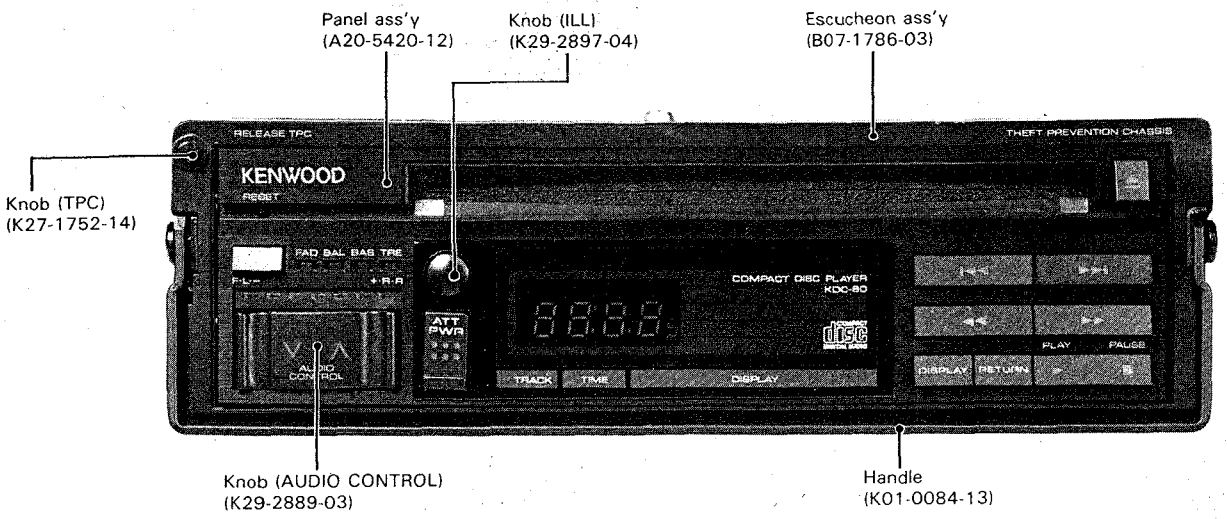

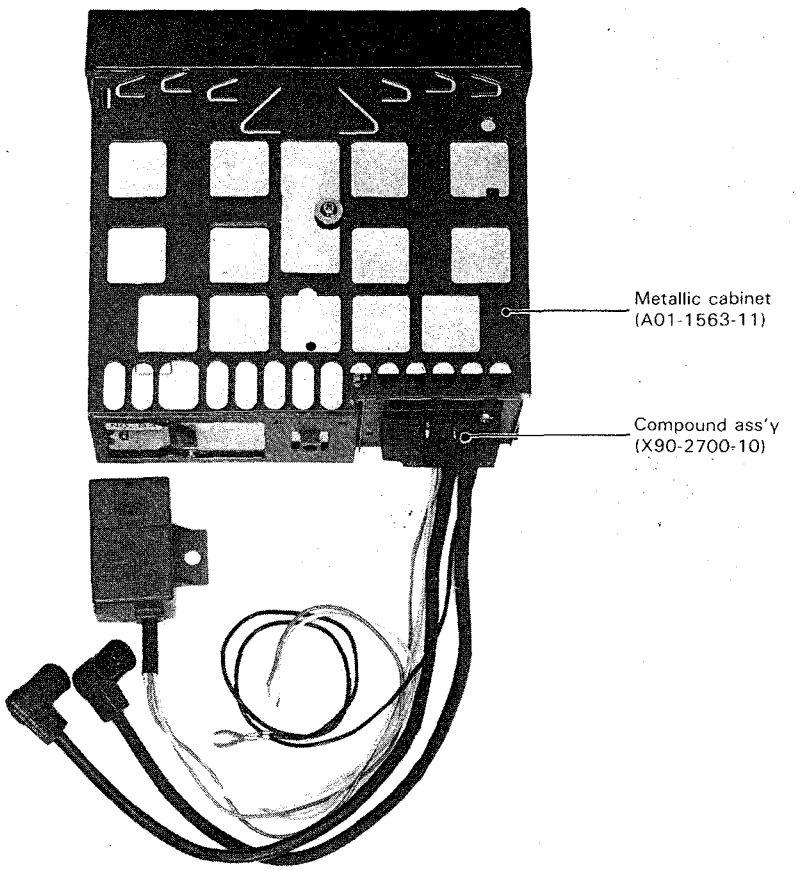

CAUTION
Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

* Refer to parts list on page 78.

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SERVICING NOTES

NOTES ON HANDLING THE OPTICAL PICK-UP BLOCK OR BASE UNIT

The laser diode in the optical pick-up block may suffer electrostatic breakdown because of the potential difference generated by the charged electrostatic load, etc. on clothing and the human body.

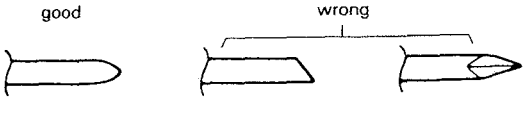
During repair, pay attention to electrostatic breakdown and also use the procedure in the printed matter which is included in the repair parts.

The flexible board is easily damaged and should be handled with care.

Flexible Circuit Board Repairing

1. Keep the temperature of the soldering iron at 270° ±10°C during repairing.
   You can maintain the temperature of the soldering iron around 270°C by using the thermal controller as illustrated on the right.
2. Do not touch the soldering iron more than 4 seconds or 3 times on the same conductor of the circuit board.
3. Do not apply force on the conductor when soldering or unsoldering.

Tip of soldering iron



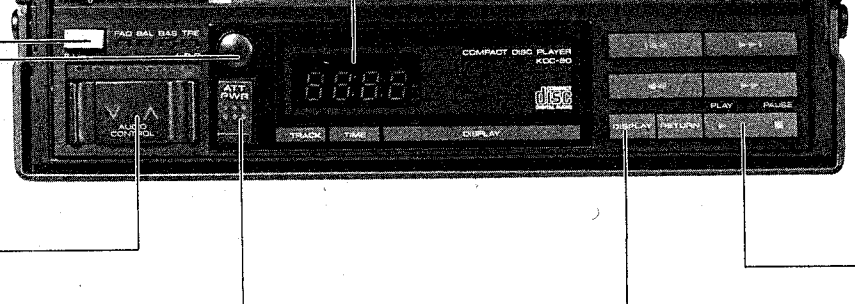
[CD]: Switch function or display during Compact Disc player operation.

Audio switch
When this switch is pressed, the fader, balance, bass or treble can be adjusted using the ∧ / ∨ switch.

Reset button
When the installation and all the wiring is finished, press this button.
Not usually used however, when the microprocessor (micro-computer) malfunctions, press this button using a sharp-pointed object. When this button is pressed, the unit is reset to its initial state. Therefore, all the memories and clock needs to be adjusted.

Display window
When play starts, the track No. is displayed first, and the elapsed playing time will be displayed shortly thereafter.
By pressing the Display switch, the display content can be switched to the track No. or elapsed playing time.
When the end of disc is attained by holding the ▷▷ switch, "– –" appears on the display. In this case, press the ⏮ or ◁◁ switch to return to the digit display.

Disc slot
Insert a compact disc with its label surface facing up. The disc is then automatically loaded into the unit and play will start.



Illumination switch
This switch is used to select the illumination, Green or Orange.

Eject switch
Press to eject the disc.

Volume up (∧)/down (∨) switch
Used for volume adjustment. These switches are also used to adjust the fader, balance, bass or treble.

Power/Attenuator switch
When this switch is pressed momentarily, the Volume indicator blinks and the volume level instantaneously drops by −20 dB. When this switch is pressed again, the indicator goes off and the previous volume level resumes.

When this switch is pressed for more than 2 seconds, power is turned OFF.

Display switch
Each time this switch is pressed in CD play mode, the display shows the track number or elapsed playing time.

Play/Pause switch
When a disc is loaded, the unit automatically enters the play mode and the ▷ indicator lights.
To suspend play temporarily, press this switch. The □ indicator will light.
To resume playback, press the switch again. The play re-starts from the position when it was suspended.

Switch function or display during Compact Disc player operation.

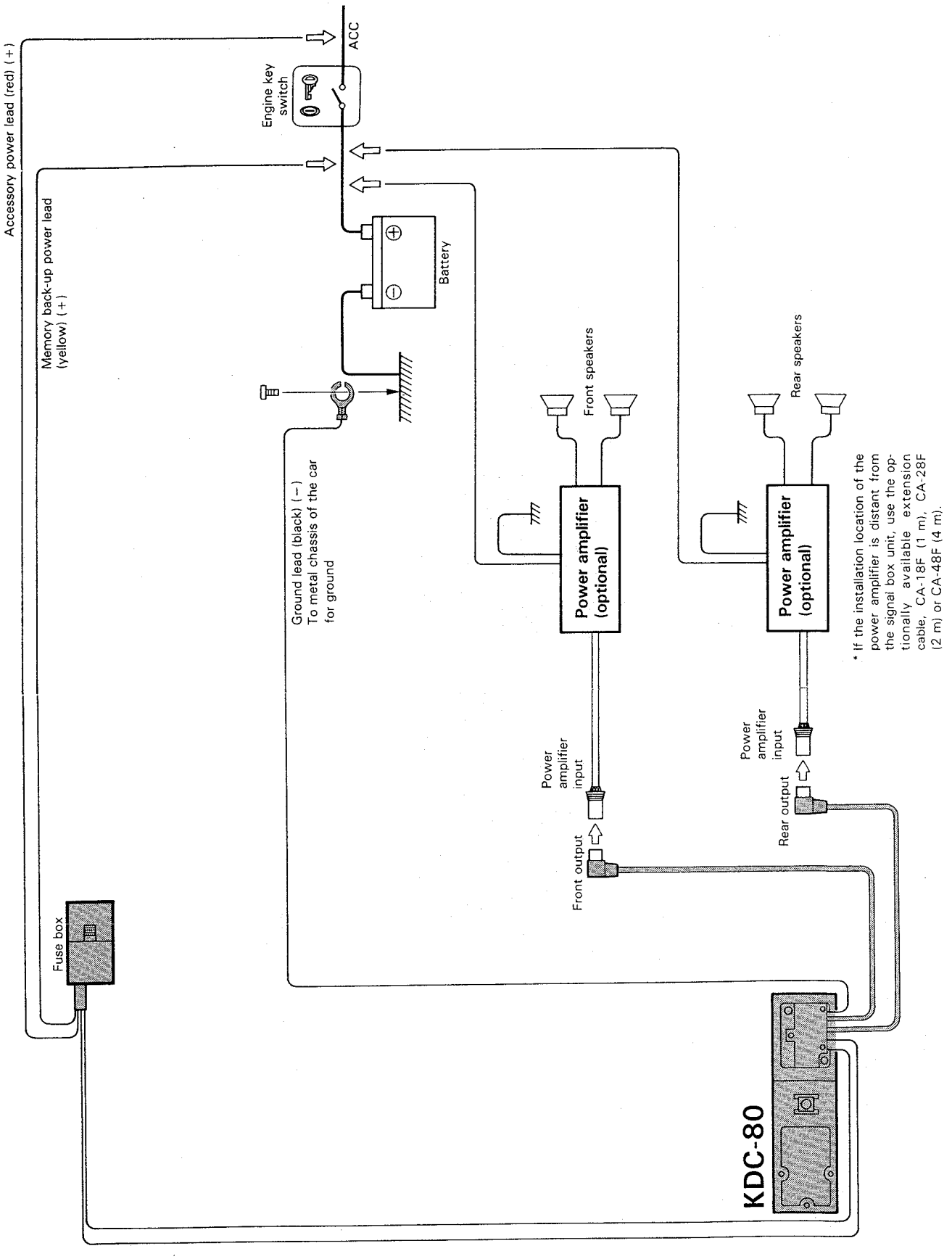
Volume level indicator
Displays the volume level. This also displays the position when adjusting the fader, balance, bass or treble.

Music search switches
During CD play, press either side of this switch to start playback at the beginning of a particular selection.
⏮: To go back to the beginning of a previous selection.
⏭: To skip ahead to the beginning of a later selection.

Search switches
During CD play, press either side of this switch to search for a particular point on the disc.
⏪: To go backwards at high speed.
⏩: To skip ahead at high speed.

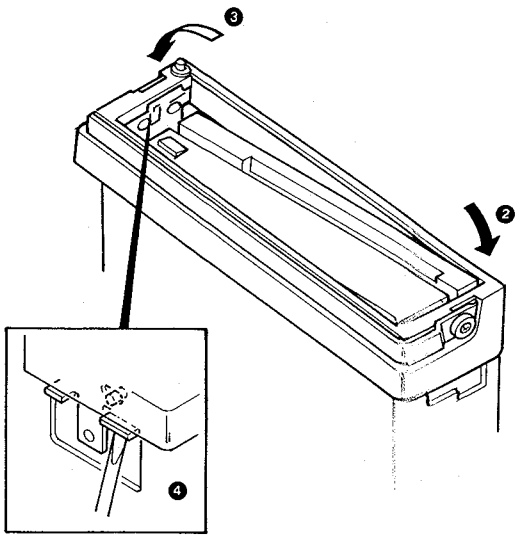
Return switch
When this switch is pressed during CD play, the unit starts playback at the beginning of the disc.

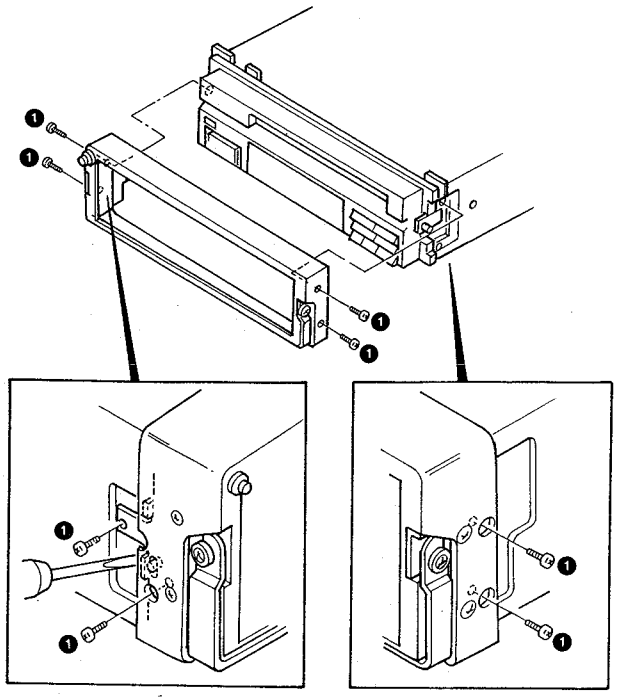
CONNECTION


Accessory power lead (red) (+)
Memory back-up power lead (yellow) (+)
Engine key switch
ACC
Battery
Ground lead (black) (–)
To metal chassis of the car for ground
Front speakers
Rear speakers
Power amplifier (optional)
Power amplifier (optional)
Power amplifier input
Power amplifier input
Front output
Rear output
Fuse box
KDC-80
* If the installation location of the power amplifier is distant from the signal box unit, use the optionally available extension cable, CA-18F (1 m), CA-28F (2 m) or CA-48F (4 m).

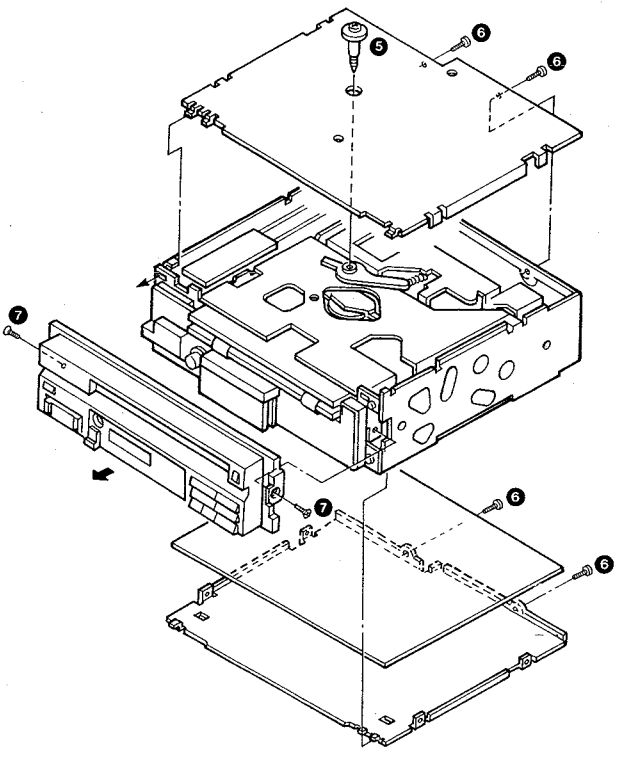
DISASSEMBLY FOR REPAIR

1. Remove the metal fittings and the four screws (❶) located on the side panels.
   Using a flat-blade screwdriver, release the bosses located on the side panels, and remove the escutcheon.
2. Assembling the escutcheon.
   First, stand the main body, with its side panel down, on the table.
   Mount the escutcheon to the bosses on the right side panel (❷).
3. Mount the escutcheon to the bosses on the left side panel (❸).
4. When inserting the metal fitting into the bosses of the left side panel, lift the metal fitting using a flat-blade screwdriver (❹).



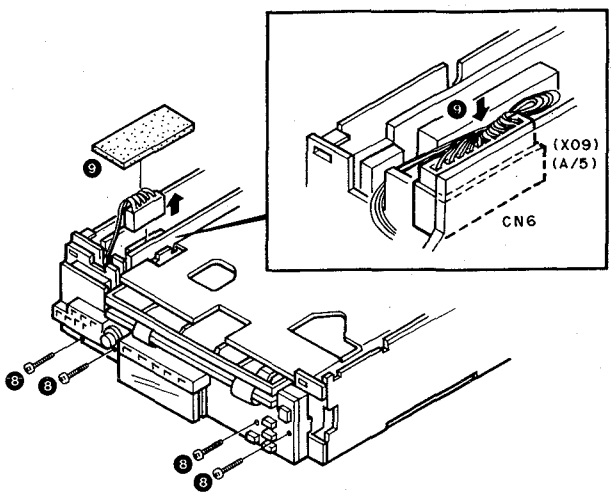


5. Remove the shipping screw (❺).
6. Remove the four screws (❻) on the top cover, bottom cover and on the rear panel.
7. Remove the two flat-head screws (❼) on the front panel and on the sub-chassis, then pull out the front panel toward the front.

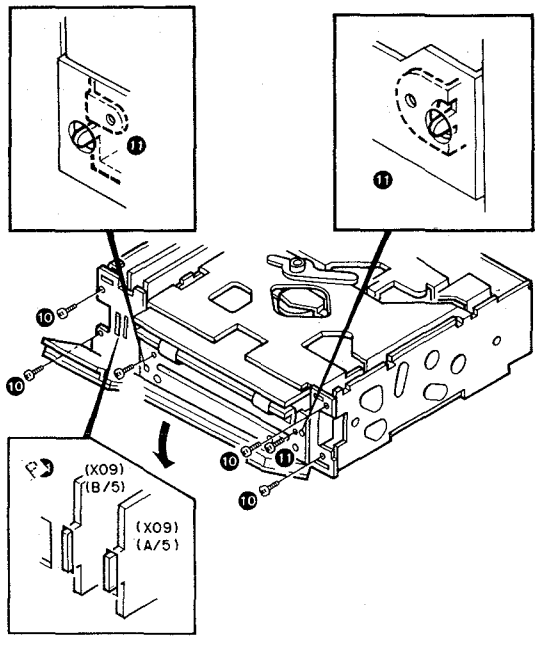


DISASSEMBLY FOR REPAIR

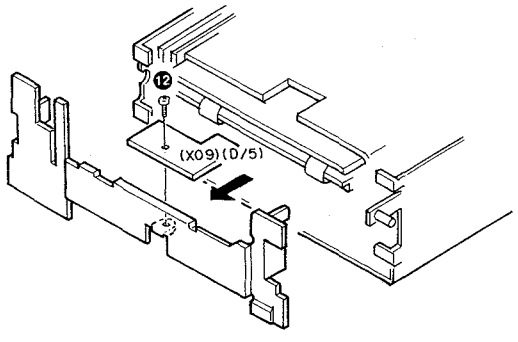
8. Remove the four screws (❽) retaining the (X25-3190) board.
9. Remove the foam rubber spacer (❾) mounted in-between the (X09) (A/5) and (X09) (A/5) boards.
   Remove the CN6 connector connected to the (X09) (B/5) board.
   Precautions on re-installing the CN6 connector:
   The wires should be inserted into the clearance between IC1 on the (X09) (B/5) board and the CN6 connector. If the wires protrude, the top cover may not fit correctly.



10. Hold down the (X25-3190) PC board in the direction of the arrow, and then remove the four screws (❿) retaining the sub-chassis and on the (L) and (R) side panels.
11. Remove the two screws retaining the sub-chassis and on the mechanism. When re-installing, insert the lugs into the holes of the sub-chassis (⓫). Insert the lugs of the (X09) (A/5) and (B/5) boards into the holes of the sub-chassis (⓫).

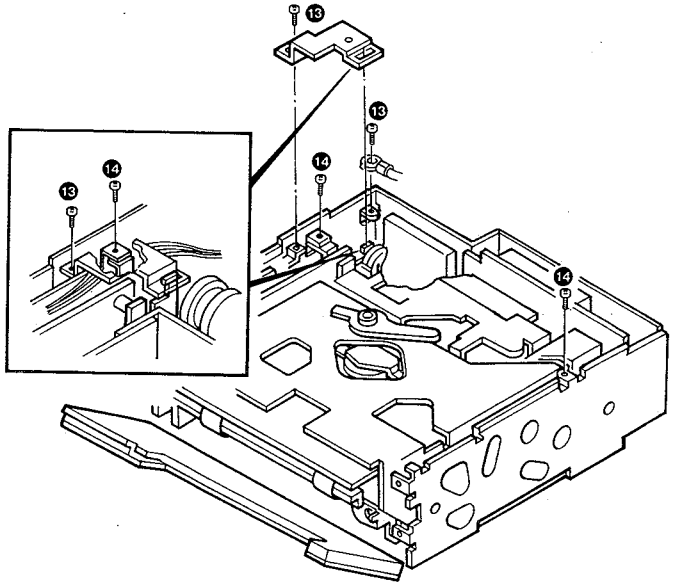


12. Remove the screw (⓬) retaining the sub-chassis and the (X09) (D/5) board.

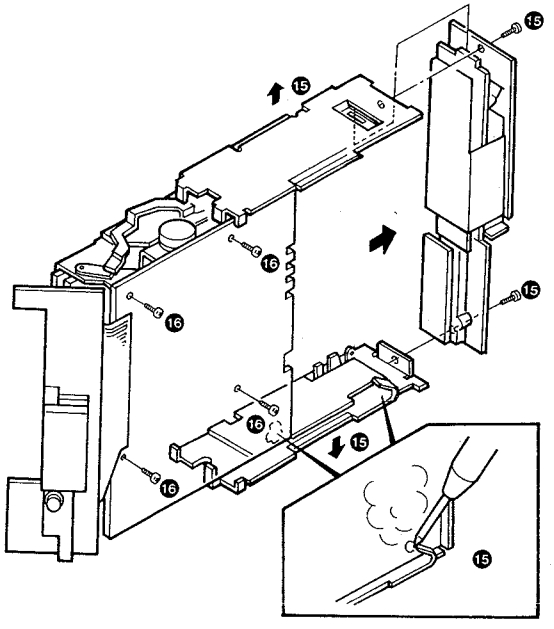


DISASSEMBLY FOR REPAIR

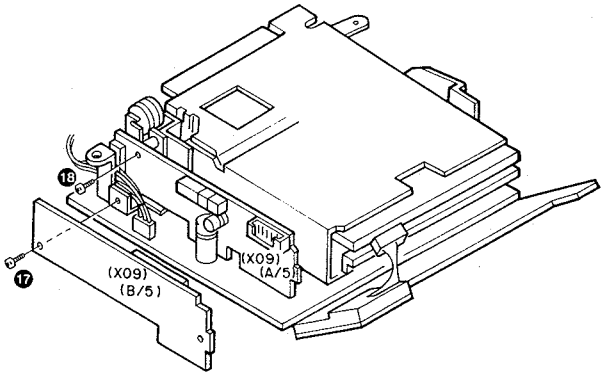
13. Remove the screws (⑬) retaining the (L) side panel and the cord clamper.
    Remove the screw (⑬) retaining the (L) side panel and the lug terminal.
    Remove the screw (⑬) retaining the rear panel and the lug terminal.
14. Remove the two screws (⑭) retaining the mechanism and the (L) and (R) side panels.



15. Stand the main body, with its side panel down, on the table.
    Heat and remove the solder on the side panel (L) and on the mother PC board. (⑮)
    Remove the two screws (⑮) retaining the (L) and (R) side panels and on the rear panel to remove them.
16. Remove the four screws (⑯) retaining the mother PC board and on the mechanism.

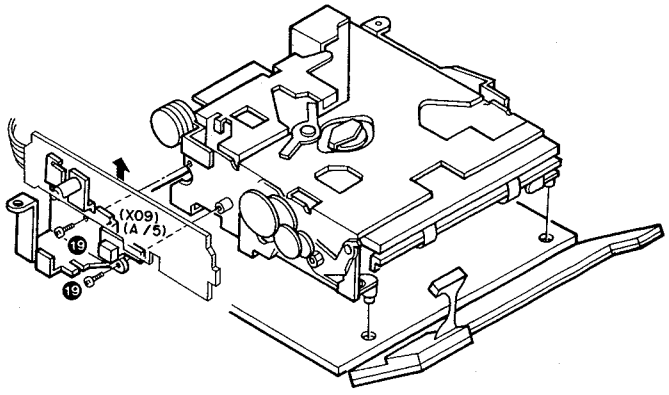


17. Remove the screw (⑰) retaining the (X09) (B/5).
18. Remove the screw (⑱) retaining the (X09) (A/5).



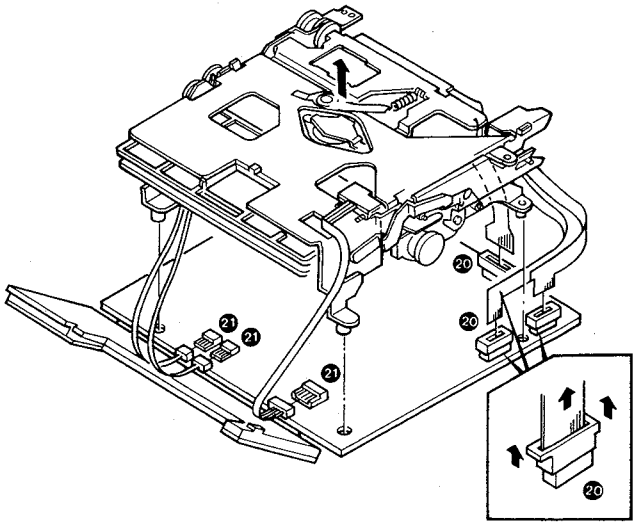
DISASSEMBLY FOR REPAIR

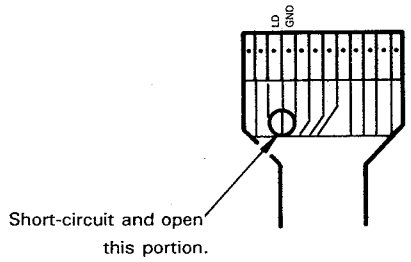
19. Slide the (X09) (A/5) PC board upward.
Remove the two screws (⑲) retaining the mechanism and PC board metal fitting.



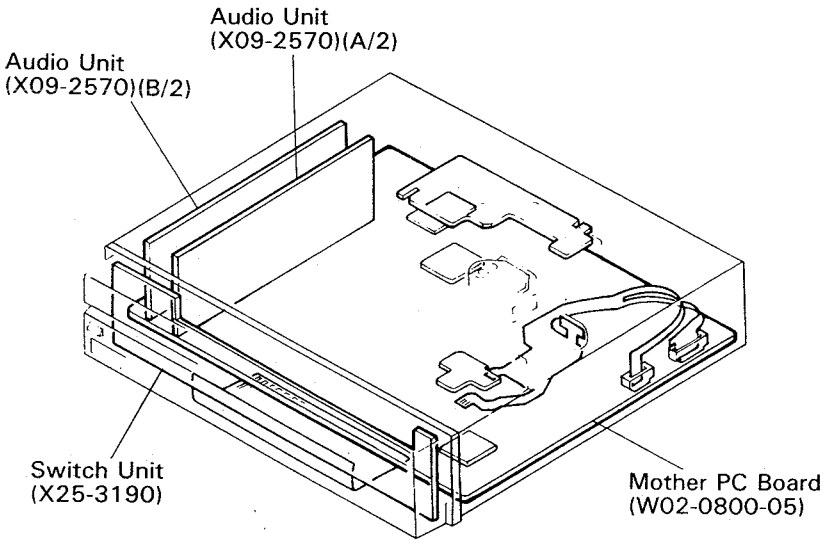
20. Remove the CNP501 to CNP503 connectors (⑳) connected to the mechanism and the mother PC board.
21. Remove the CNP504 to CNP506 connectors (㉑).
Then remove the mechanism in the direction of the arrow.

Note:
- **Be sure to short-circuit the pattern on the flexible circuit board as shown in the drawing below after removing it from the CNP501 (in order to prevent electrostatic breakage).**
- **Prior to assembling the CNP501, be sure to open the shortcircuited pattern.**





Printed circuit board layout

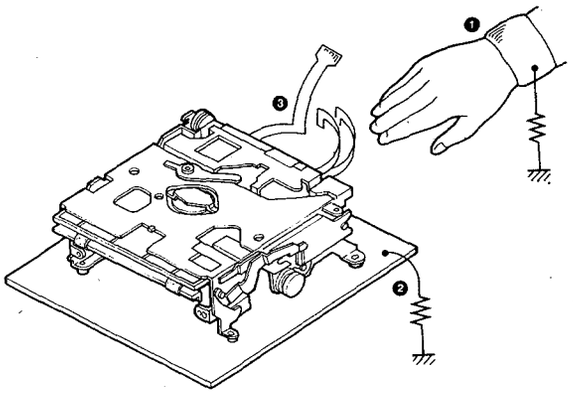


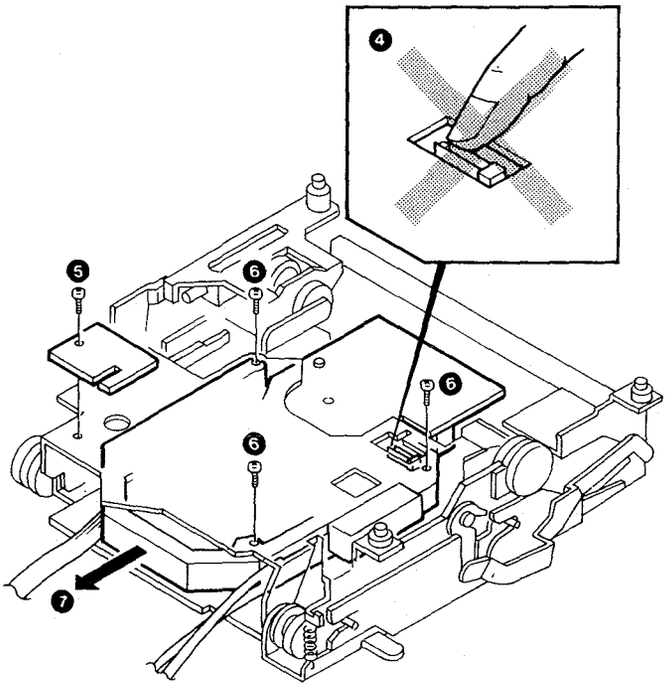
DISASSEMBLY FOR REPAIR

Handling the mechanism deck, and pickup section removal

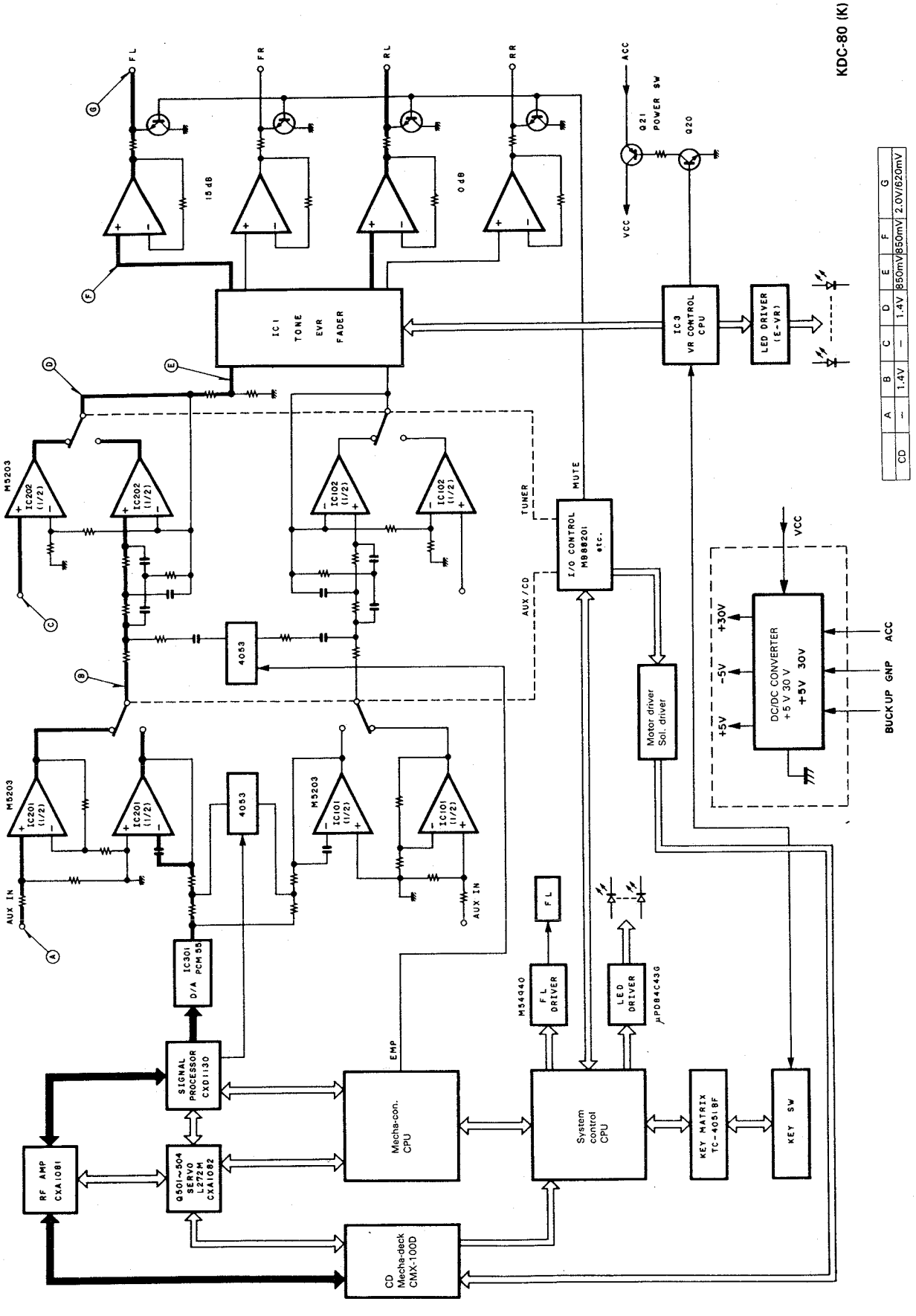
1. **Grounding of the human body (service personnel)**
   To ground the static electricity charge on your body, be sure to wear a grounded wrist band (less than 10^8 ohms). The static electricity charge on your clothes won't be grounded via the grounded wrist band, so make sure that your clothes do not touch the mechanism deck.

2. **Grounding of the operation table**
   Be sure to spread a conductive sheet (less than 10^8 ohms) or copper plate on the place where the mechanism deck is to be put, and also ground it.
3. Do not apply excessive force to the flexible printed circuit board. It may be damaged or cut.
   Especially when peeling off adhesive tape, pay special attention to the board.
4. If you touch the limit switches of the optical block, the precisely adjusted sled (feed) section could be damaged. Be careful not to touch the limit switches.
5. Remove the screw retaining the LED board to remove it.
6. Remove the three screws retaining the pickup section.
7. Pull out the pickup section in the direction of the arrow.





BLOCK DIAGRAM

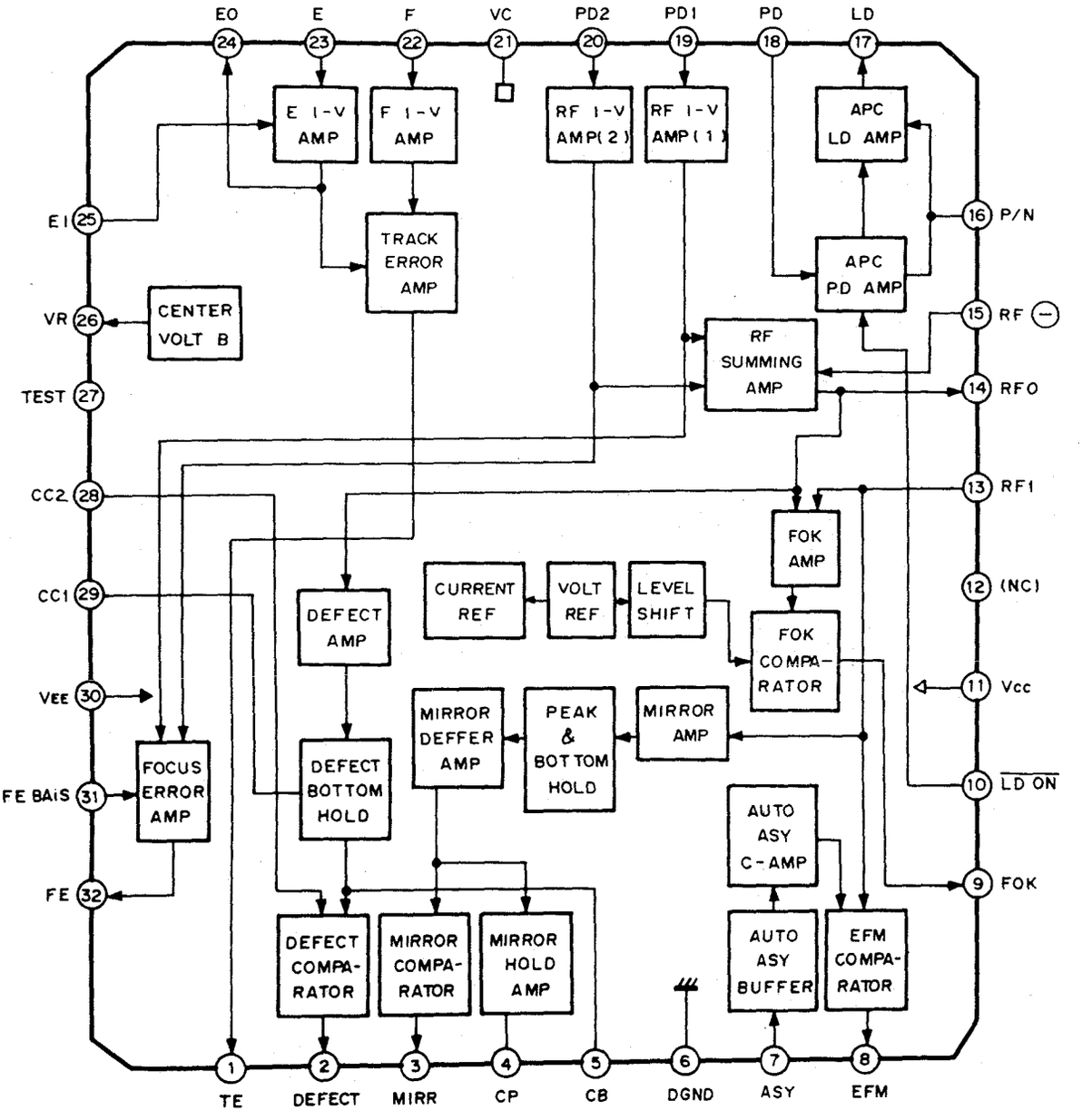


CIRCUIT DESCRIPTION

IC501: CXA1081Q RF amplifier

The CXA1081Q supplies the following functions as required for controlling the RF amp in the compact disc player.

- RF amp
- Focusing error amp
- Tracking error amp
- APC circuit
- Auto asymmetry control amp
- Focus OK detection circuit
- Mirror detection circuit
- Defect detection circuit
- EFM comparator



CIRCUIT DESCRIPTION

Explanation of terminals

Terminal No.	Terminal name	I/O	Function
1	TE	O	Tracking error amp output pin.
2	DEFECT	O	Defect comparator output pin. (DC voltage: connected to a 10 kΩ load).
3	MIRR	O	Mirror compartor output pin. (DC voltage: connected to a 10 kΩ load).
4	CP	I	Mirror hold capacitro output pin. Mirror comparator non-invert input.
5	CB	I	Defect bottom hold capacitor connect pin.
6	DGND	—	Connected to GND when using a positive (+)/negative (−) dual-voltage power supply. Connected to GND (V_{EE}) when using a single-voltage power supply.
7	ASY	I	Auto asymmetry control input pin.
8	EFM	O	EFM comparator output pin. (DC voltage: connected to a 10 kΩ load).
9	FOK	O	FOK comparator output pin. (DC voltage: connected to a 10 kΩ load).
10	$\overline{\text{LD ON}}$	I	LD ON/OFF select pin. (DC voltage: when LD ON).
11	Vcc	—	Positive power supply.
13	RFI	I	Input pin of the C-coupled signal output from the RF summing amp.
14	RFO	O	Check point of eye pattern for the RF summing amp output pin.
15	RF ⊖	I	RF summing amp feedback input pin.
16	P/N	I	P-sub/L-sub select pin of LD. (DC voltage: in N-sub mode)
17	LD	O	APC LD amp output pin. (DC voltage: PD open in N-sub mode)
18	PD	I	APC PD amp input pin. (DC voltage: open)
19	PD1	I	RF I-V amp (1) invert input pin. Current input by connecting to PIN diode A+C.
20	PD2	I	RF I-V amp (2) invert input pin. Current input by connecting to PIN diode B+D.
21	VC	—	Connected to GND when using a positive (+)/negative (−) dual-voltage power supply. Connected to VR (pin 14) when using a single-voltage power supply.
22	F	I	F I-V amp invert input pin. Current input by connecting to PIN diode F.
23	E	I	E I-V amp invert input pin. Current input by connecting to PIN diode E.
24	EO	O	E I-V amp output pin.
25	EI	I	E I-V amp feedback input pin. For E I-V amp gain adjustment.
26	VR	O	DC voltage ouput pin of $(V_{CC}+V_{EE})/2$.
27	TEST	—	Open
28	CC2	I	Input pin of the C-coupled signal output from the defect bottom hold.
29	CC1	O	Defect bottom hold output pin.
30	V_{EE}	—	Connected to the negative power supply when using a positive (+)/negative (−) dual-voltage power supply. Connected to GND when using a single-voltage power supply.
31	FE BIAS	I	Bias pin at the focus error amp non-invert side. For CMR adjustment of the focus error amp.
32	FE	O	Focus error amp output pin.

CIRCUIT DESCRIPTION

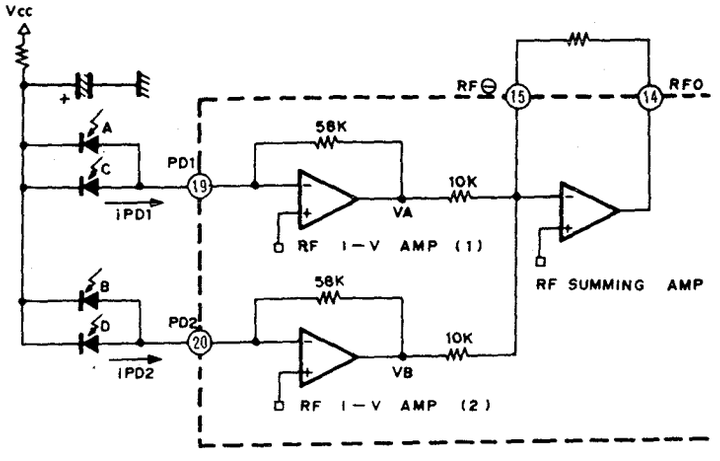
Explanation of function

- **RF amp**

The photodiode current input to the input pins (PD1, PD2) is converted to a voltage by an equivalent resistance of 58kΩ in RF I–V amp (1) and (2) respectively. The voltage which is converted from the current of the photodiode (A + B + C + D) is added in the RF summing amp and is output from the RFO pin. The eye pattern can be checked at this pin.

The low frequency component of the RFO output voltage, V_{RFO} is represented by the following equation:

$$V_{RFO} = 2.2 \times (V_A + V_B)$$
$$= 127.6k\,\Omega \times (i_{PD1} + i_{PD2})$$



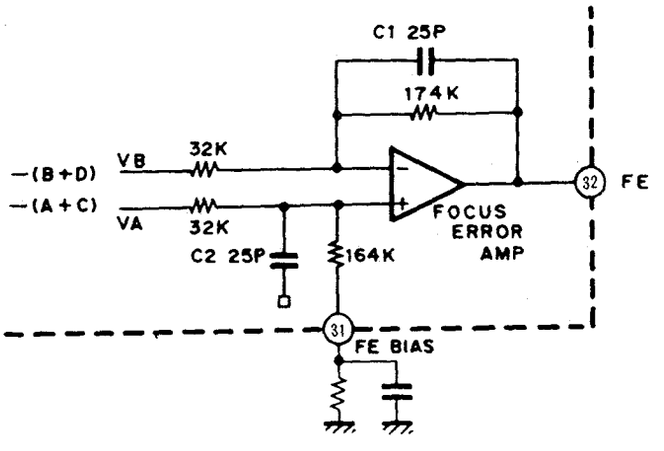
RF I–V amplifier

- **Focus error amp**

The difference between the RF I–V amp (1) output (VA) and the RF I–V amp (2) output (VB) is calculated, and the current of the photodiode (A + C – B – D) is converted to a voltage and output.

The FE output voltage (low frequency) is represented by the following equation:

$$V_{FE} = 5.4 \times (V_A - V_B)$$
$$= (i_{PD2} - i_{PD1}) \times 315.4k\,\Omega$$



CIRCUIT DESCRIPTION

- **Tracking error amp**

The current from the side spot photodiodes is input to pins E and F and is converted to a voltage by the E I–V amp and F I–V amp respectively. That is:

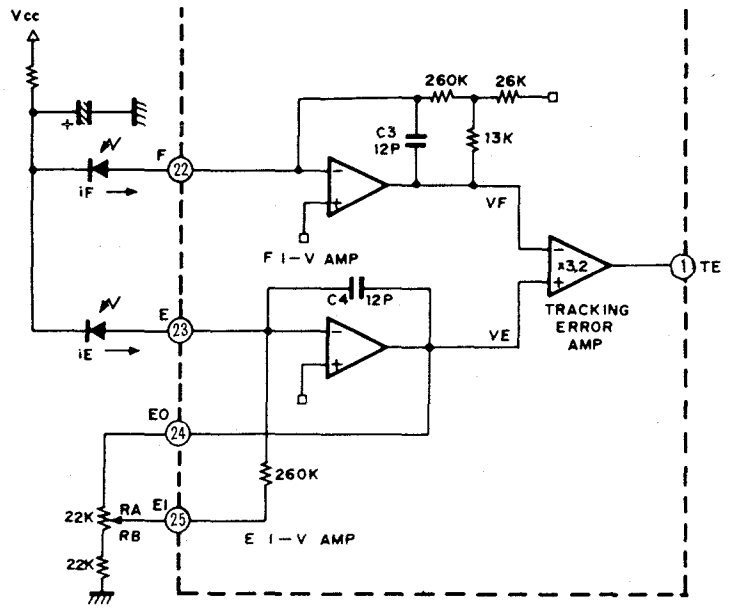
$$V_F = iF \times 403k\,\Omega$$

$$V_E = iE \times 260k\,\Omega \times R_A/(R_B + 22k) + (R_A + 260k)$$

The difference between the E I–V amp and the F I–V amp is calculated by the tracking error amp, and the photodiode (E–F) current is converted to a voltage and output.

$$V_{TE} = (V_E - V_F) \times 3.2$$

$$= (iE - iF) \times 1290k\,\Omega$$



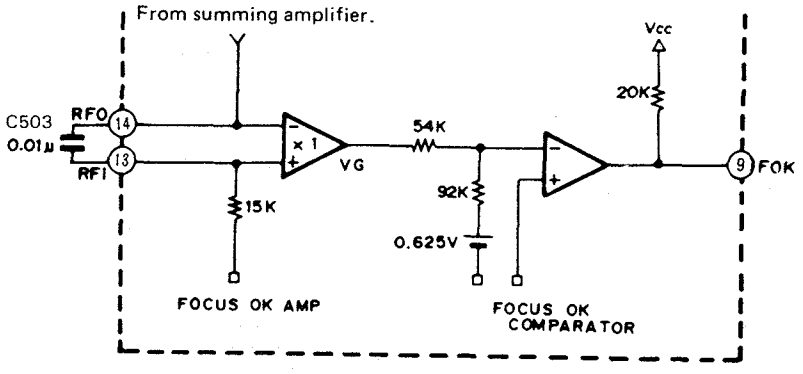
- **Focus OK circuit**

The focus OK circuit creates a timing window, turning the focusing servo ON with the focus search status.

While the RF signal is present at pin 2, its HPF output is present at pin 1. At the same time, the LPF output (opposite phase) of the focus OK amp is obtained.

The focus OK output is inverted when $V_{RFI} - V_{RFO} \fallingdotseq -0.37V$.

C503 is used to determine the time constants of the EFM comparator, the HPF in the mirror circuit, and the LPF in the focus OK amp. Normally, C503 = 0.01μF is selected, with fc = 1kHz. This will prevent degradation of the block error rate due to an RF envelope lack caused by cracks, etc. on the disc.



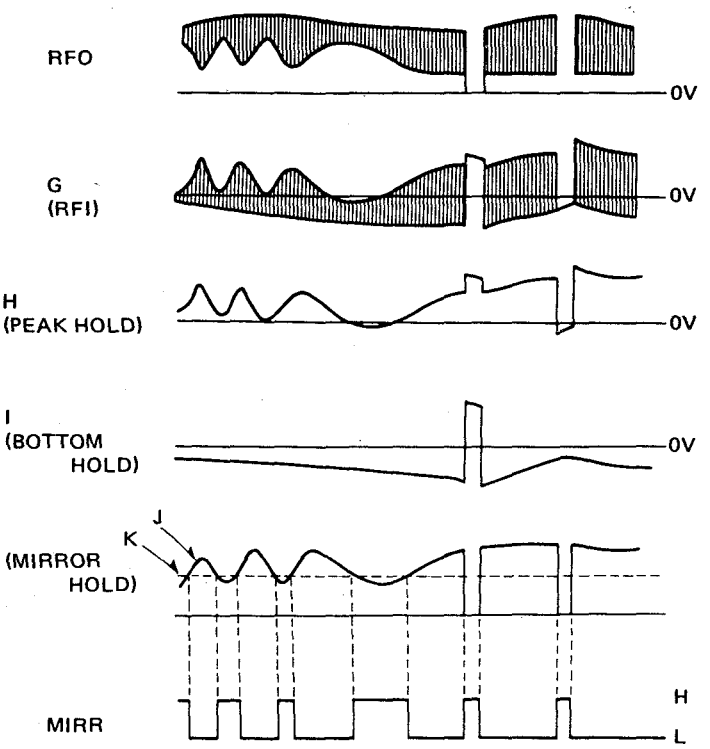
CIRCUIT DESCRIPTION

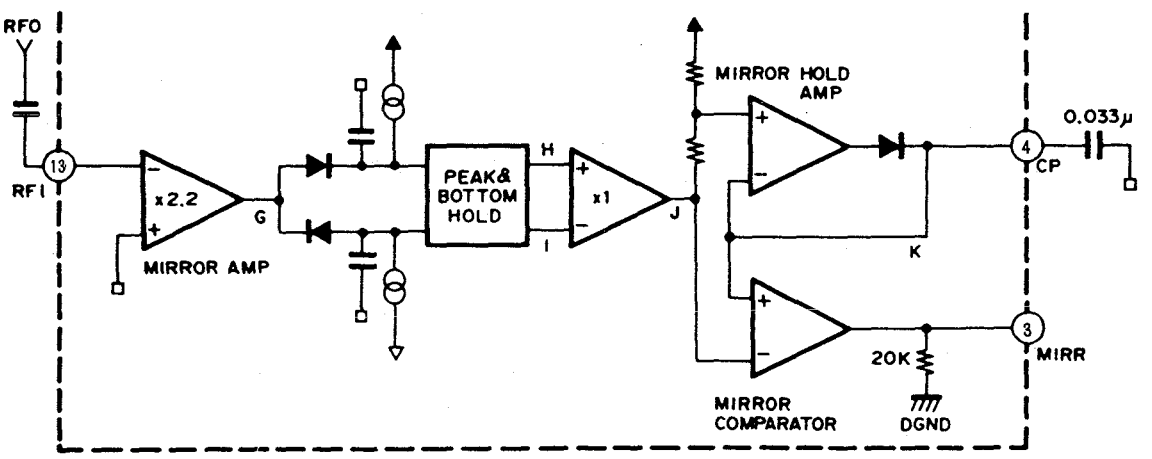
- **Mirror circuit**

In the mirror circuit, after the RFI signal is amplified, both peak and bottom holds are held by a time constant which can follow a traverse of 30kHz, while only the bottom hold is held by a time constant which can follow a cyclic period envelope variation respectively.

These peak/bottom hold signals, H and I are differentially amplified to obtain the DC-reproduced envelope signal J.

This signal is compared with signal K, that the 2/3 level of the peak value is peak held by a large time constant so that the mirror output is obtained. That is, the mirror output goes "L" on the disc tracks and goes "H" between tracks (mirror section). In addition, the output goes "H" when a defect is detected. The time constant of the mirror hold should be quite larger when compared with the traverse signal.





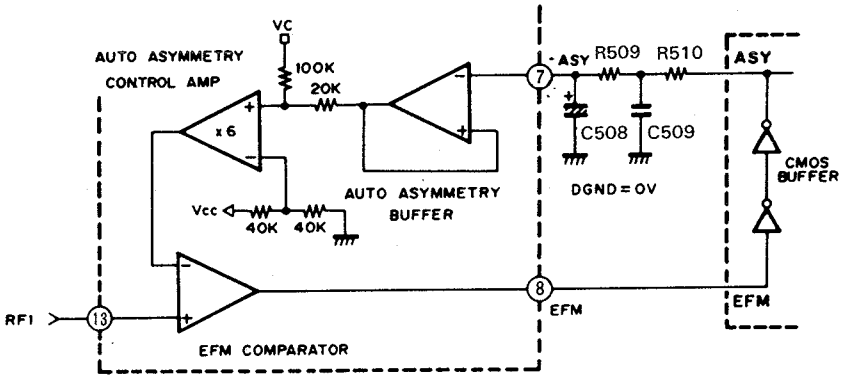
CIRCUIT DESCRIPTION

- **EFM comparator**

The EFM comparator converts the RF signal into a binary coded signal. Since asymmetry caused by dispersion when manufacturing the discs cannot be reduced by AC coupling only, the reference voltage of the EFM comparator is controlled using the characteristics that the present probability of a 1 or 0 is 50% each for the binary coded EFM signal.

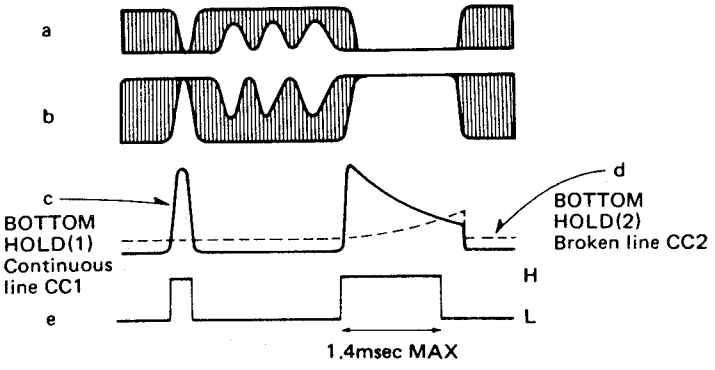
The EFM comparator is designed as a current switching type, and the "H" and "L" levels are not equal to the power voltages. Therefore, feedback is required via a CMOS buffer.

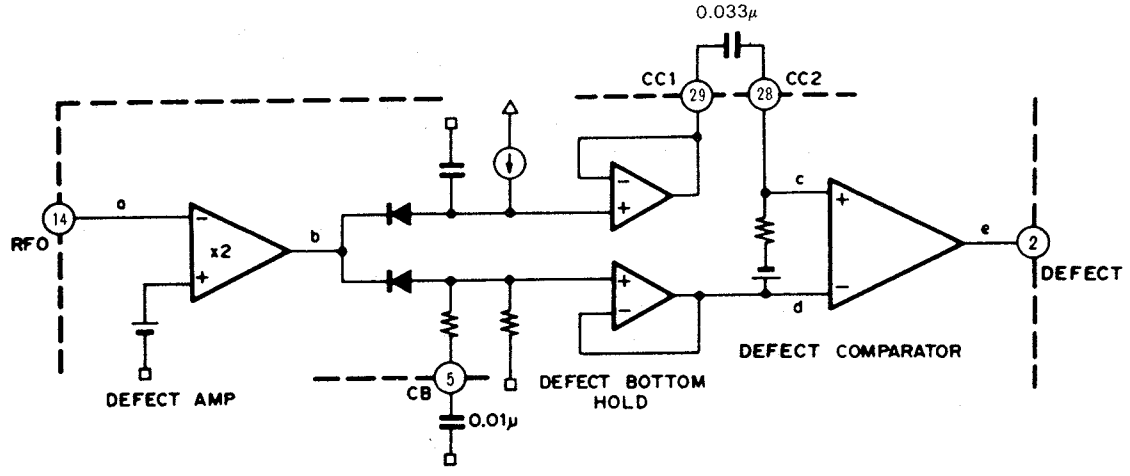
R509, R510, C508 and C509 constitute a LPF to obtain the DC component of (Vcc + DGND)/2 (V). If the cut-off frequency (fc) is set to more than 500Hz, leakage of the EFM low frequency signals will be greatly increased and will result in a degradation of the block error rate.



- **Defect circuit**

After inverting the RFI signal, the defect circuit bottom holds with the two long/short time constants. The bottom hold with a shorter time constant responds to a mirror defect of more than 0.1msec on the disc, and the bottom hold with a longer time constant holds the mirror level obtained immediately before the defective section. These signals are C-coupled, then differentiated with level shifting. The signals are compared with each other to generates the mirror defect detecting signals.





CIRCUIT DESCRIPTION

IC502: CXA1082AQ Servo signal processor for the CD

General

The CXA1082AQ is a bipolar IC developed for servo control in Compact Disc players.

Features

- Operates on a signal +5 V power supply as well as on a ±5 V dual-voltage power supply.
- Low power consumption (165 mW with ±5 V, 100 mW with +5 V).
- Same servo function as CX20108 (focusing, tracking, sled servo)
- Built-in auto sequencer.
- Built-in spindle servo LPF.
- Built-in loop filter and VCO for an EFM clock generating PLL.
- A minimum of external parts required.
- Sled overrun prevention circuit.
- Disc defect treatment circuit.
- Anti-shock circuit
- Linear motor feed for high-speed access.
- Shared use of a serial data bus with the CX23035 and CXD1135Q.
- The microprocessor and software both have upward compatibility with the CX20108.
- The pulse height of the focusing search, track jump, and sled kick can be set with externally connected resistors.

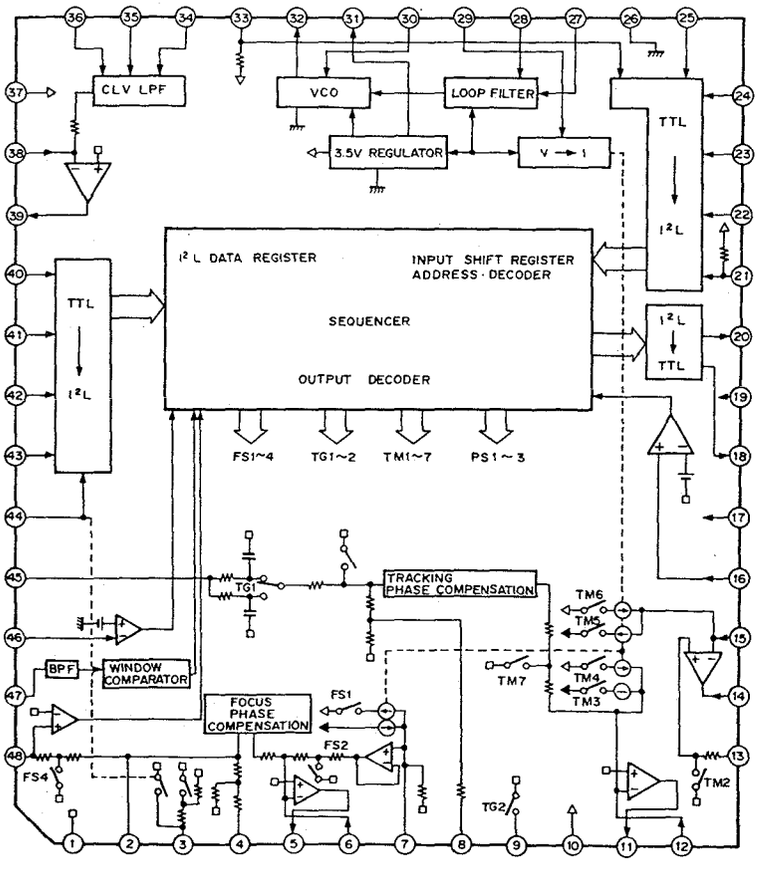
Functions

- Focusing servo control
- Tracking servo control
- Sled servo control
- Spindle servo
  Low Pass Filter, drive amplifier
- EFM clock generating PLL
  Loop filter: 8.64 MHz VCO
- Auto sequencer
  Incorporating a RAM

Structure

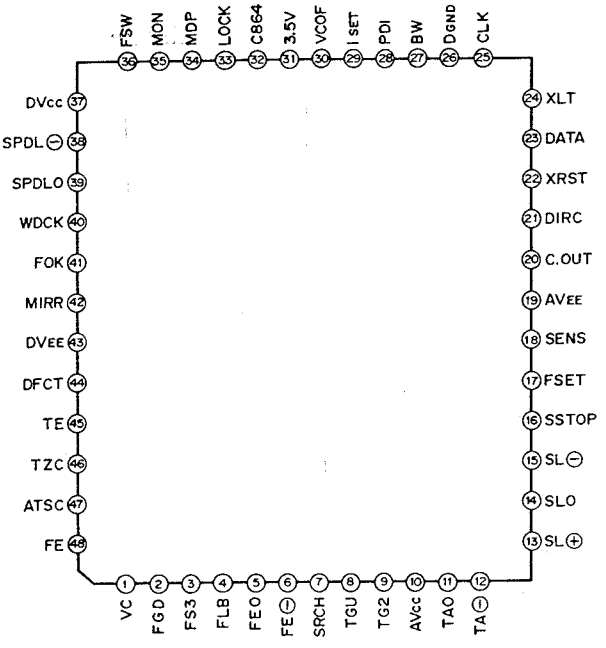
Bipolar silicon monolithic IC

Block diagram



CIRCUIT DESCRIPTION

Pin configuration

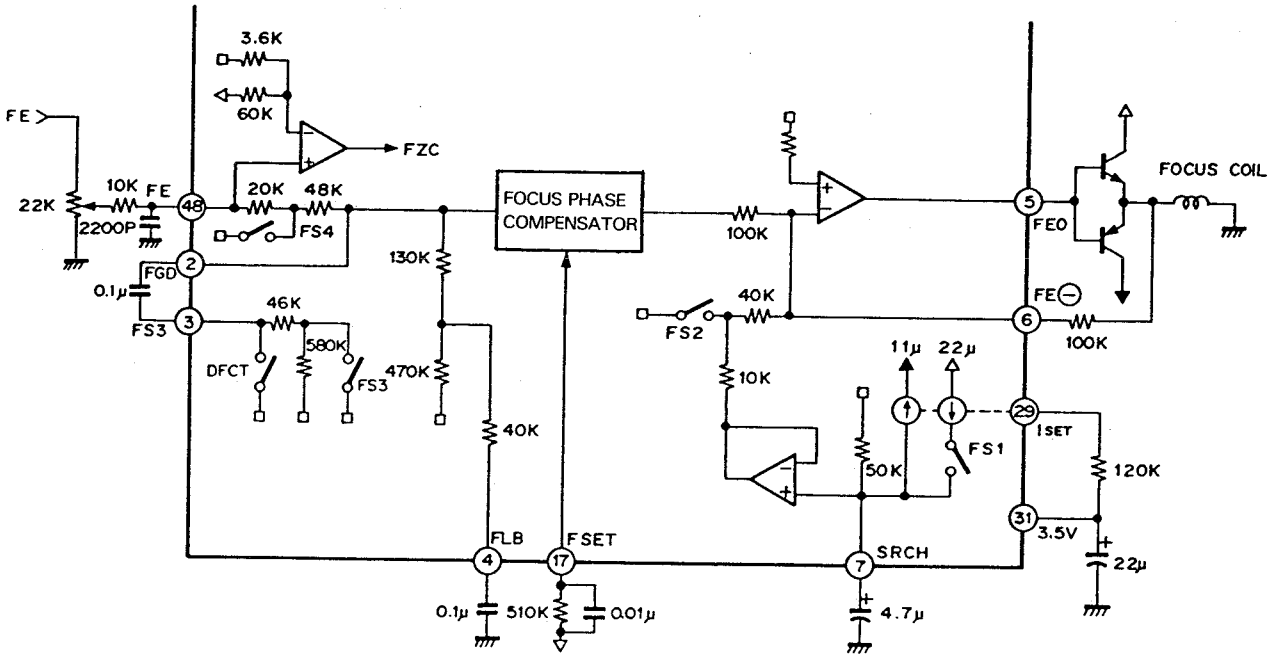


Terminal explanations

Terminal No.	Terminal name	Function
2	FGD	To lower the high frequency gain of the focus servo, insert a capacitor between this pin and pin 3.
3	FS3	The high frequency gain of the focus servo is selected by switching FS3 ON/OFF.
4	FLB	Time constant external connect pin, for boosting the focus servo low frequencies.
5 11 14 39	FEO TAO SLO SPDLO	Power transistor drive op amplifier output pins.
6	FE⊖	Focus amplifier inverted input pin.
7	SRCH	Time constant external connect pin, for creating the focus search waveform.
8	TGU	Time constant external connect pin, for selecting the tracking high frequency gain.
9	TG2	Time constant external connect pin, for selecting the tracking high frequency gain.
12	TA⊖	Tracking amplifier inverted input pin.
13	SL⊕	Sled amplifier non-inverted input pin.
15	SL⊖	Sled amplifier inverted input pin.
16	SSTOP	Limit switch ON/OFF detection signal input pin, for detecting the innermost edge of the disc.
17	FSET	Setting pin for the focus tracking phase peak value compensation, and fo of the CLV LPF.
18 20	SENS C.OUT	Output pins for an interface with a microprocessor.
21 22 23 24 25 33	DIRCT XRST DATA XLT CLK LOCK	Input pins for an interface with a microprocessor. A 47-kohm pull-up resistor is only incorporated in pins 21 and 33.
27	BW	Loop filter time constant external connect pin.
28	PDI	Input pin for the phase comparator output PDO of CXD23035/CXD1135.
29	ISET	Inputs a current which determines the level of the focus search, track jump, and sled kick.
30	VCOF	The self-advancing frequency of the VCO is almost proportional to the resistance between this pin and pin 31.
32	C864	8.64 MHz VCO output pin.
34	MDP	CXD23035/CXD1135 MDP pin connect pin.
35	MON	CXD23035/CXD1135 MON pin connect pin.
36	FSW	LPF time constant external connect pin, for the CLV servo error signal.
38	SPDL⊖	Spindle drive amplifier inverted input pin.
40 41 42 44	WDCK FOK MIRR DFCT	Input pins for an interface with a microprocessor.
45	TE	Tracking error signal input pin.
46	TZC	Tracking zero-cross comparator input pin.
47	ATSC	Window comparator input pin for ATSC detection.
48	FE	Focusing error signal input pin.

CIRCUIT DESCRIPTION

Focusing servo system



This block diagram is of the focusing servo system.

When FS3 is ON, the capacitor connected between pins 2 and 3 and the internal resistance determines the low-frequency time constant which can attenuate the high-frequency gain.

The capacitor between pin 4 and GND determines the time constant for boosting the low frequencies in normal playback.

The peak frequency of the focusing phase compensation is inversely proportional to the resistance connected to pin 17, and the frequency is about 1.2 kHz when the resistance is 510 k-ohms.

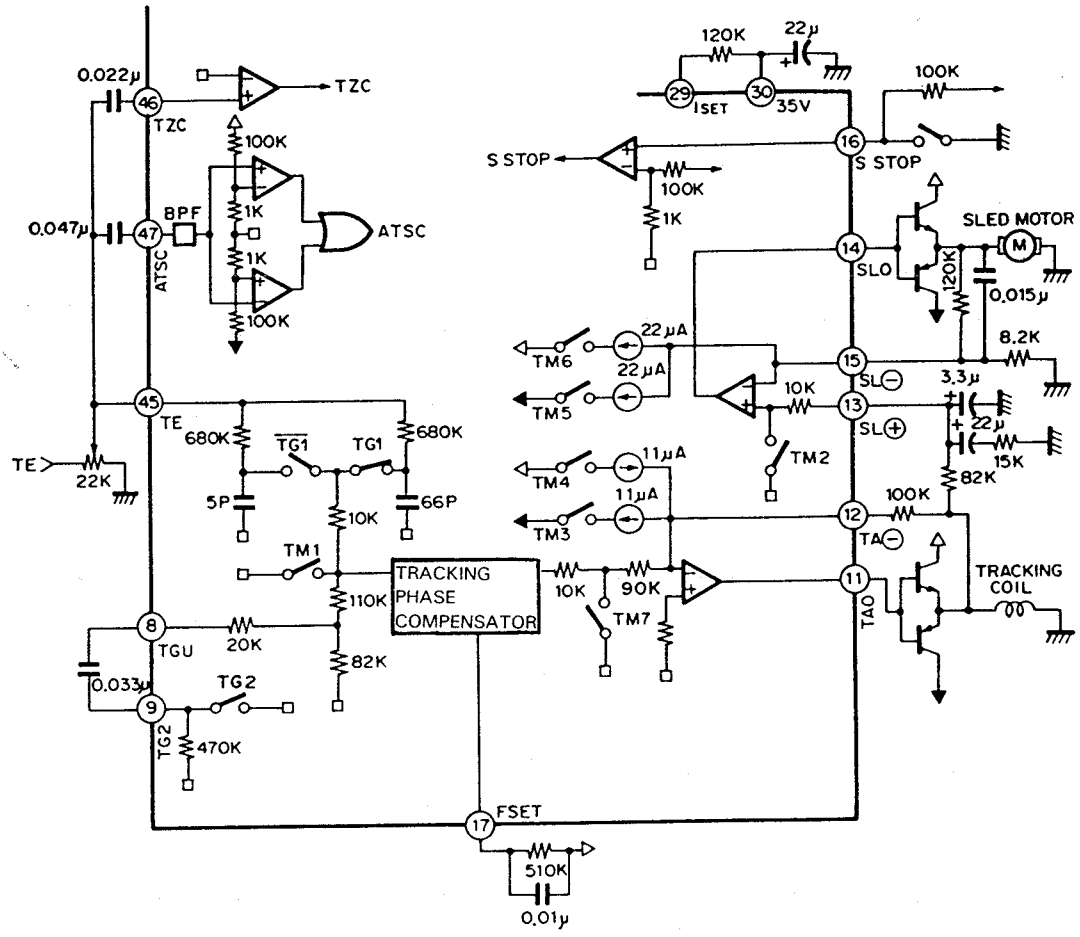
The focus search level is about ±1.1 Vp-p with these constants. The level is inversely proportional to the value of the resistance connected between pins 29 and 30. Note that the track jump and sled kick levels are also varied by changing this resistance.

The level has been set to 5.7% of the difference between Vcc, the inverted input reference voltage of the FZC comparator, and VC (pin 1); i.e. (Vcc − VC) × 5.7%.

* Varying the value of resistance connected to pin 17 also varies the phase compensation peak values of focusing/tracking/sled servos and fc of the CVL LPF. At the same time, the op amplifier's dynamic range and offset voltage are also varied.

CIRCUIT DESCRIPTION

Tracking and sled servo system



This block diagram is of the tracking and sled servo system. The capacitor connected between pins 8 and 9 determines the time constant for attenuating the high-frequency gain. The peak frequency for the tracking phase compensation is inversely proportional to the resistance connected to pin 17, and the frequency is about 1.2 kHz when the resistance is 510 k-ohms.

A FWD or REV tracking jump is performed by switching TM3 or TM4 ON. At this time, the peak voltage applied to the tracking coil depends on the current at TM3 or TM4 and the feedback resistance through pin 12, as shown by the following equation:

Track jump peak voltage = TM3 (TM4) current × Feedback resistance

A FWD or REV sled kick is performed by switching TM5 or TM6 ON. At this time, the peak voltage applied to the sled motor depends on the current at TM5 or TM6 and the feedback resistance through pin 15, as shown by the following equation.

Sled jump peak voltage = TM5 (TM6) current × Feedback resistance

The currents at these switches are determined by the resistance connected between pins 29 and 31. When the value is 120 k-ohms, the currents are:

±11 μA at TM3 and TM4, and

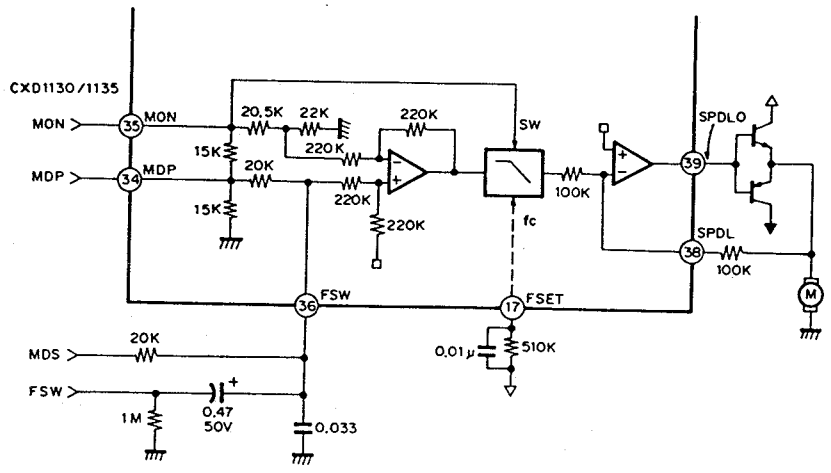
±22 μA at TM5 and TM6.

The currents are inversely proportional to the resistance, and the variable range is from about 5 to 40 μA with TM3.

S STOP is the signal used to detect the ON/OFF of the limit switch for detecting the innermost position for the linear motor.

CIRCUIT DESCRIPTION

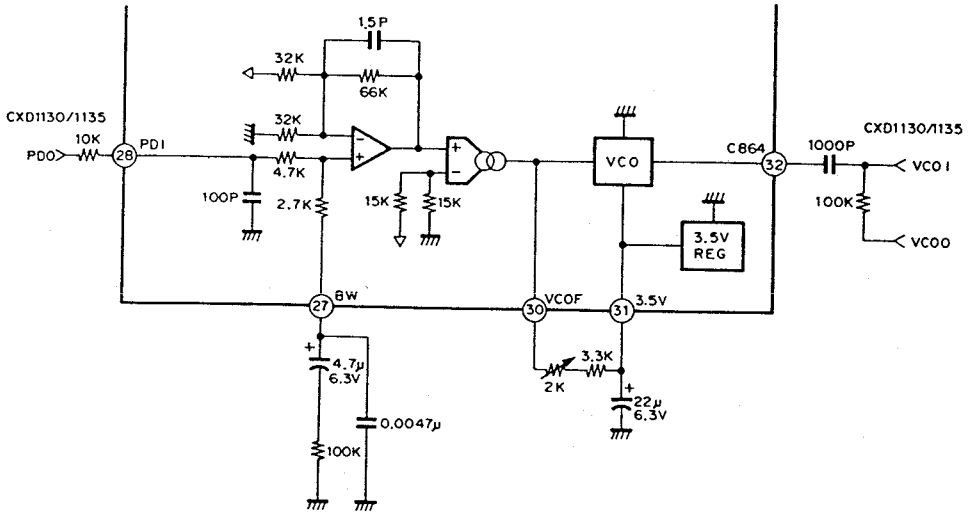
Spindle servo and LPF circuitry



The carrier component in the CLV servo error signals MDS and MDP are eliminated by a two-stage LPF, which consists of a 200 Hz LPF formed by a 0.033 μF capacitor and a 20 k-ohms resistor connected to pin 36 and an internal LPF (fc up to 200 Hz when 510 k-ohms is connected to pin 17).

In the CLV-S mode, FSW becomes L, and fc of the LPF at pin 36 drops to enhance the filtering effect. The resistor connected to pin 17 need not be stabilized but only connected to Vcc, because its fc will not be varied by supply voltage variation.

VCO loop filter and 8.64 MHz VCO circuitry



The phase comparator output, PDO, is input via pin 28, sent through the loop filter to eliminate the PWM carrier component, then V-I converted, and added with the self-advancing frequency set current from pin 30 for use in controlling the VCO frequency. The VCO's self-advancing frequency is almost proportional to the resistance connected between pins 30 and 31. The value of this resistance is set so that the PLL capture range center is 4.3218 MHz at CXD1135/1130 pin 70. The external circuit connected to pin 27 BW is used to maximize the capture range during accessing, so that access is possible even when the self-advancing frequency deviates due to the VCO's temperature characteristic, etc.

CIRCUIT DESCRIPTION

IC503: CXD1130Q Digital signal processing LSI for the CD

General

The CXD1130Q is a digital signal processing LSI for a Compact Disc player, and has the following functions.

1. Bit clock reproduction by an EFM-PLL circuit
2. EFM data demodulation
3. Frame sync signal detection, protection and insertion
4. Powerful error detection and correction
5. Interpolation with an average value, or by holding the previous value
6. Demodulation of a sub code signal, error detection of a sub code Q
7. Spindle motor CLV servo
8. 8-bit tracking counter
9. CPU interface with a serial bus
10. Sub code Q register
11. Digital filter

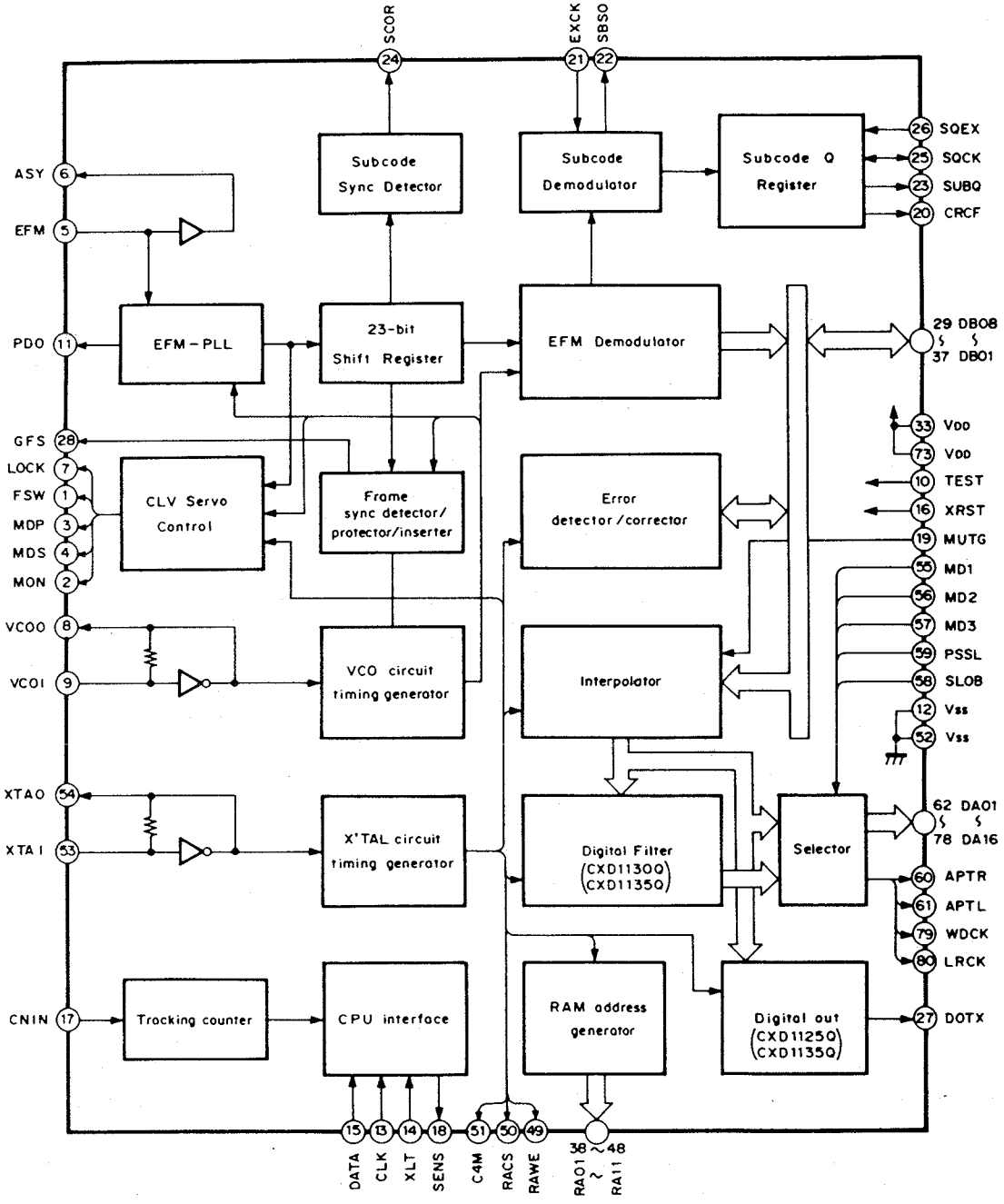
Features

- All digital signals used in playback can be processed using only a single chip.
- An aperture-correction digital filter is built in.

Structure

CMOS IC

Block diagram



CIRCUIT DESCRIPTION

Terminal explanations

Terminal No.	Terminal name	I/O	Function
1	FSW	O	Time constant switching output of output filter of spindle motor.
2	MON	O	ON/OFF control output of spindle motor.
3	MDP	O	Drive output of spindle motor. Rough speed control in CLV-S mode and phase control in CLV-P mode.
4	MDS	O	Drive output of spindle motor. Speed control in CLV-P mode.
5	EFM	I	EFM signal input from RF amplifier.
6	ASY	O	Output for controlling the slice level of EFM signal.
7	LOCK	O	Samples the GFS signal with WFCK/16, and outputs "H" when the level is high. When it is "L" for eight times, in arrow, outputs "L".
8	VCOO	O	VCO output. f = 8.6436 MHz when locked to EFM signal.
9	VCOI	I	VCO input.
10	TEST	I	(0 V)
11	PDO	O	Phase comparison output of EFM signal and VCO/2.
12	V_{SS}	—	GND (0 V)
13	CLK	I	Serial data transmission clock input from CPU. Data is latched at rising edge of a clock.
14	XLT	I	Latch input from CPU. Data (serial data from CPU) from the 8 bit shift register is latched in each register.
15	DATA	I	Serial data input from CPU.
16	XRST	I	System reset input. Reset at "L".
17	CNIN	I	Input of tracking pulse.
18	SENS	O	Output of internal status in correspondence to the address.
19	MUTG	I	Muting input. In the case when ATTM of internal register A is "L". Normal status when MUTG is "L" or soundless state when it is "H".
20	CRCF	O	Output of result of CRC check of sub code Q.
21	EXCK	I	Clock input for sub code serial output.
22	SBSO	O	Sub code serial output.
23	SUBQ	O	Sub code Q output.
24	SCOR	O	Sub code sync S0 + S1 output.
25	SQCK	I/O	Sub code Q read-off clock.
26	SQEX	I	SQCK select input.
27	DOTX	O	DIGITAL OUT output. (Outputs the $\overline{\text{WFCK}}$ signal when CXD1130Q or D0 is off)
28	GFS	O	Display output of frame sync lock status.
29	DB08	I/O	Data pin of external RAM. DATA8 (MSB)
30	DB07	I/O	Data pin of external RAM. DATA7
31	DB06	I/O	Data pin of external RAM. DATA6
32	DB05	I/O	Data pin of external RAM. DATA5
33	V_{DD}	—	Power supply (+5 V)
34	DB04	I/O	Data pin of external RAM. DATA4
35	DB03	I/O	Data pin of external RAM. DATA3
36	DB02	I/O	Data pin of external RAM. DATA2
37	DB01	I/O	Data pin of external RAM. DATA1 (LSB)
38	RA01	O	Address output of external RAM. ADDR01 (LSB)
39	RA02	O	Address output of external RAM. ADDR02
40	RA03	O	Address output of external RAM. ADDR03
41	RA04	O	Address output of external RAM. ADDR04
42	RA05	O	Address output of external RAM. ADDR05
43	RA06	O	Address output of external RAM. ADDR06

CIRCUIT DESCRIPTION

Terminal No.	Terminal name	I/O	Function
44	RA07	O	Address output of external RAM. ADDR07
45	RA08	O	Address output of external RAM. ADDR08
46	RA09	O	Address output of external RAM. ADDR09
47	RA10	O	Address output of external RAM. ADDR10
48	RA11	O	Address output of external RAM. ADDR11 (MSB)
49	RAWE	O	Write Enable signal output to external RAM. (Active at "L").
50	RACS	O	Chip select signal output to external RAM. (Active at "L").
51	C4M	O	Crystal dividing output. f= 4.2336 MHz.
52	V_{SS}	—	GND (0 V).
53	XTAI	I	Crystal oscillator input. f=8.4672 MHz or 16.9344 MHz depending on the mode selected.
54	XTAO	O	Crystal oscillator output. f=8.4672 MHz or 16.9344 MHz depending on the mode selected.
55	MD1	I	Mode select input 1.
56	MD2	I	Mode select input 2.
57	MD3	I	Mode select input 3.
58	SLOB	I	Audio data output code select input. 2's complement output when "L", offset binary output when "H".
59	PSSL	I	Audio data output mode select input. Serial output when "L", parallel output when "H".
60	APTR	O	Aperture compensation control output. "H" when R-ch.
61	APTL	O	Aperture compensation control output. "H" when L-ch.
62	DA01	O	DA01 (parallel audio data LSB) output when PSSL="H", C1F1 output when PSSL="L".
63	DA02	O	DA02 output when PSSL="H", C1F2 output when PSSL="L".
64	DA03	O	DA03 output when PSSL="H", C2F1 output when PSSL="L".
65	DA04	O	DA04 output when PSSL="H", C2F2 output when PSSL="L".
66	DA05	O	DA05 output when PSSL="H", C2FL output when PSSL="L".
67	DA06	O	DA06 output when PSSL="H", C2PO output when PSSL="L".
68	DA07	O	DA07 output when PSSL="H", RFCK output when PSSL="L".
69	DA08	O	DA08 output when PSSL="H", WFCK output when PSSL="L".
70	DA09	O	DA09 output when PSSL="H", $\overline{\text{PLCK}}$ output when PSSL="L".
71	DA10	O	DA10 output when PSSL="H", UGFS output when PSSL="L".
72	DA11	O	DA11 output when PSSL="H", GTOP output when PSSL="L".
73	V_{DD}	—	Power supply (+5 V).
74	DA12	O	DA12 output when PSSL="H", RAOV output when PSSL="L".
75	DA13	O	DA13 output when PSSL="H", C4LR output when PSSL = "L".
76	DA14	O	DA14 output when PSSL="H", $\overline{\text{C21O}}$ output when PSSL="L".
77	DA15	O	DA15 output when PSSL="H", C21O output when PSSL="L".
78	DA16	O	DA16 (parallel audio data MSB) output when PSSL="H", DATA output when PSSL="L".
79	WDCK	O	Strobe signal output. 176.4 kHz when DF is ON, 88.2 kHz with CXD1125Q or when DF is OFF.
80	LRCK	O	Strobe signal output. 88.2 kHz when DF is ON, 44.1 kHz with CXD1125Q or when DF is OFF.

Notes:

C1F1 :
C1F2 : Error correction status monitor output for C1 decode.

C2F1 :
C2F2 : Error correction status monitor output for C2 decode.

C2FL : Correction status output. Goes "H" when the currently corrected C2 series data cannot be corrected.

C2PO : C2 pointer signal. Synchronized to the audio data output.

RFCK : Read frame clock output. 7.35 MHz when locked to the crystal line.

WFCK : Write frame clock output. 7.35 MHz when locked to the crystal line.

$\overline{\text{PLCK}}$: VCO/2 output. f=4.3218 MHz when locked to the EFM signal.

UGFS : Non-protected frame sync pattern output.

GTOP : Frame sync protect status display output.

RAOV : ±4 frame jitter absorption RAM overflow and underflow display output.

C4LR : Strobe signal. 352.8 kHz when DF is ON, 176.4 kHz with CXD1125Q or when DF is OFF.

$\overline{\text{C21O}}$: C21O invert output.

C21O : Bit clock output. 4.2336 MHz when DF is ON, 2.1168 MHz with CXD1125Q or when DF is OFF.

DATA : Audio signal serial data output.

CIRCUIT DESCRIPTION

Explanation of functions

1. CPU interface

(1) Data input

Each register may be set by input of 4-bit address, and 4-bit data from LSB in the timing that is shown in Fig. 1 to three pins, XLT, CLK and DATA. The address and data of each pin are as shown in Table 1, and their functions are as follows. The contents of each register become entirely 0 when XRST = "L".

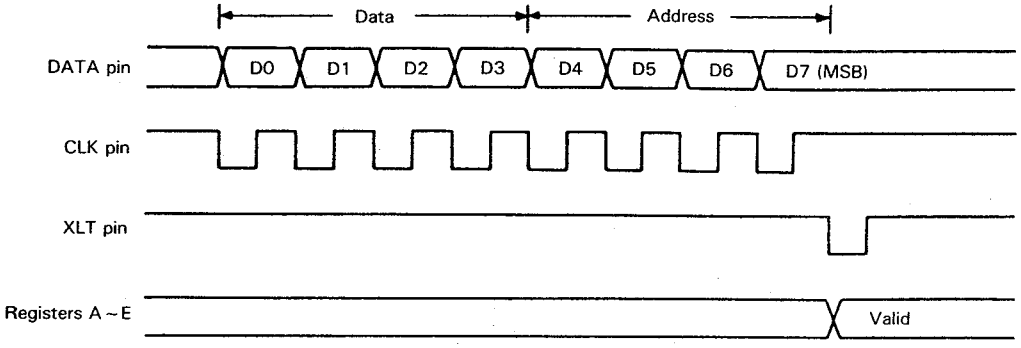


Fig. 1 Timing chart for data input

(2) Registers

Register 9 — New function control

Controls the new functions address to the CX23035.

D0 : CRCQ — Switches ON/OFF the function which outputs the CRCF data to the SUBQ pin from the rising edge of SCOR to the trailing edge of SQCK. Details are described in "**1-(5). Subcode output**". (Page 29)

D1 : NCLV — Switches between the old CLV-P servo and the new CLV-P servo by comparison with newly added base counter. Details are described in "**6. CLV servo control**". (Page 35)

D2 : HZPD — One of the defect countermeasures. Switches ON/OFF the function which makes the PDO pin a high impedance (Z) for a maximum of 0.55 ms from the trailing edge of GFS. Details are described in "**10. Countermeasures to defects**". (Page 42)

D3 : ZCMT — Switches the zero cross mute function ON/OFF. Details are described in "**7. Interpolation and mute, attenuate**". (Page 40)

Register A — Sync. protection, attenuator control

D0 : ATTM — Used for attenuating audio signals by 12 dB.

D1 : WSEL, D2 : GSEL, D3 : GSEM — Provided for switching frame sync. protection characteristics in correspondence to the time of playback and time of access. Details will be described in the paragraph of "**2. EFM demodulation**". (Page 31)

Registers B and C — Counter set, more significant 4-bit (register C) and less significant 4-bit (register B)

These registers are used for setting the tracking counter value. The data of registers B and C are preset in the counter through the 4-bit buffer register assigned by address.

Accordingly, when data of either register B or C is input, the contents of both registers are preset in the counter simultaneously as 8-bit data (either buffer register is of "OLD" data).

Register D-CLV control

D0 : GAIN — Used for setting the gain of MDP pin output in the CLV-S and CLV-H modes. It is −12 dB (time of 3/4 out of the period of RFCK/2 is of high impedance) when D0 = 0 or is 0 dB when D0 = 1.

D1 : T_P — Used for setting the period of peak hold in the CLV-S mode. Peak hold is made in the period of RFCK/4 when D1 = 0 or in the period of RFCK/2 when D1 = 1.

D2 : T_B — Used for determining the period of bottom hold in the CLV-S and CLV-H modes. Bottom hold is made in the period of RFCK/32 when D2 = 0 or in the period of RFCK/16 when D2 = 1.

D3 : DIV — Used for setting the frequency dividing ratio of RFCK, WFCK in the CLV-P mode. When D3 = 0, phase comparison of RFCK/4 and WFCK/4 is made, and output is made out of MDP pin in each case.

CIRCUIT DESCRIPTION

Register E — CLV mode

It is as shown in Table 1.

The details of each mode will be described in "**6. CLV servo control**". (Page 37)

D3 to D0 are all "0" when XRST = L.

Register name	Command	Address D7 ~ D4	Data				SENS pin
			D3	D2	D1	D0	
9*1	New function control	1001	ZCMT	HZPD	NCLV	CRCO	Z
A*2	Sync protection attenuator control	1010	GSEM	GSEL	WSEL	ATTM	Z
B	Counter set, Less significant 4-bit	1011	Tc3	Tc2	Tc1	Tc0	$\overline{\text{COMPLETE}}$
C	Counter set, More significant 4-bit	1100	Tc7	Tc6	Tc5	Tc4	$\overline{\text{COUNT}}$
D*3	CLV control	1101	DIV	T_B	T_P	GAIN	Z
E*4	CLV mode	1110	CLV mode				$\overline{\text{PW} \geqq 64}$

***1 Register 9**

		Dn = 0	Dn = 1
ZCMT	D3	Zero-cross MUTE off	Zero-cross MUTE on
HZPD	D2	PDO pin is always active.	PDO pin is "Z" at the trailing edge of GFS.
NCLV	D1	CLV-P servo for the frame sync signal	CLV-P servo for the base counter
CRCQ	D0	CRCF is not superimposed on SUBQ	SUBQ = CRCF at the raising edge of SCOR

***2 Register A**

GSEM	GSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	Clock
0	±3
1	±7

ATTM	MUTG pin	dB
0	0	0
0	1	−∞
1	0	−12
1	1	−12

***3 Register D**

DIV	D3	0	RFCK/4, WFCK/4	Phase comparison frequency in CLV-P mode
		1	RFCK/8, WFCK/8	
T_B	D2	0	RFCK/32	Bottom hold period in CLV-S, CLV-H mode
		1	RFCK/16	
T_P	D1	0	RFCK/4	Peak hold frequency in CLV-S mode
		1	RFCK/2	
GAIN	D0	0	−12 dB	Gain at MDP pin in CLV-S, CLV-H mode
		1	0 dB	

***4 Register E**

Mode	D3 ~ D0	MDP pin	MDS pin	FSW pin	MON pin
STOP	0000	L	Z	L	L
KICK	1000	H	Z	L	H
BRAKE	1010	L	Z	L	H
CLV-S	1110	CLV-S	Z	L	H
CLV-H	1100	CLV-H	Z	L	H
CLV-P	1111	CLV-P	CLV-P	Z	H
CLV-A	0110	CLV-S or CLV-P	Z or CLV-P	L or Z	H

Z: High impedance

Table 1 List of registers

CIRCUIT DESCRIPTION

(3) Tracking counter

This counter is provided for facilitating track jump. Load the number of tracks to be jumped in registers B and C. Count of CNIN pulses is started at rising edge of XLT after it was loaded in either register B or C.

When n (n = 256 is meant when register B = register C = 0) is loaded in registers and the address is set at "B", a signal $\overline{\text{COMPLETE}}$ that is of HIGH level up to "n" pulses and is of LOW level after "n" pulses is output of SENS pin. When the address is set at "C", signal $\overline{\text{COUNT}}$ of CNIN/2n (Hz) is output.

The tracking counter timing chart is shown in Fig. 2.

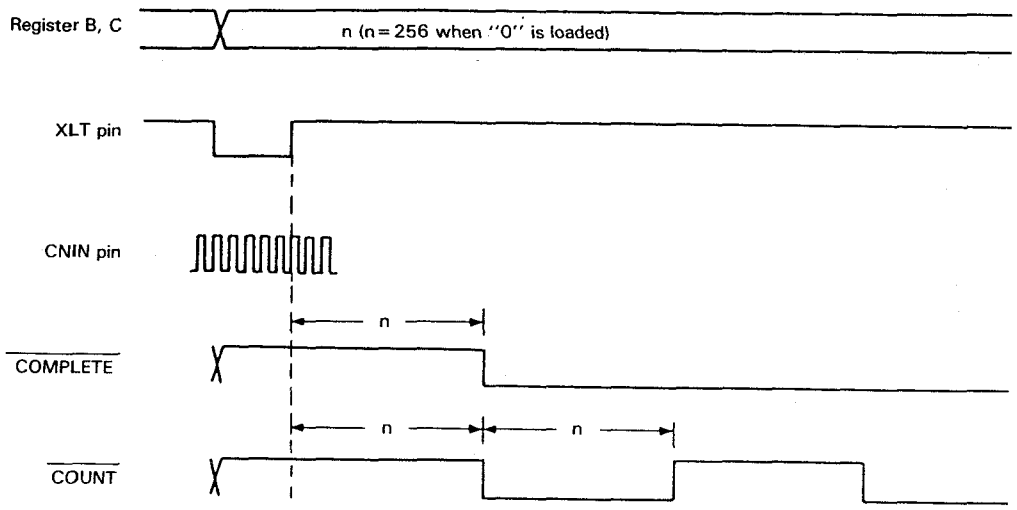


Fig. 2 Tracking counter timing chart

(4) SENS

The following signals are output from SENS pin depending on the address of D7 ~ D4.

(1) $\overline{\text{COMPLETE}}$: Address (see note) is "B"; Shown in Fig. 2.

(2) $\overline{\text{COUNT}}$: Address (see note) is "C"; Shown in Fig. 2.

(3) $\overline{\text{PW} \geqq 64}$: Address (see note) is "E"; This signal is of LOW level when the pulse width after bottom hold is over 63, and is of HIGH level otherwise. It is used for detection of a drop in the speed of the spindle motor after braking and so on.

Note: Address setting is determined by the data corresponding to D4 to D7, which are input from the DATA pins shown in Fig. 1.

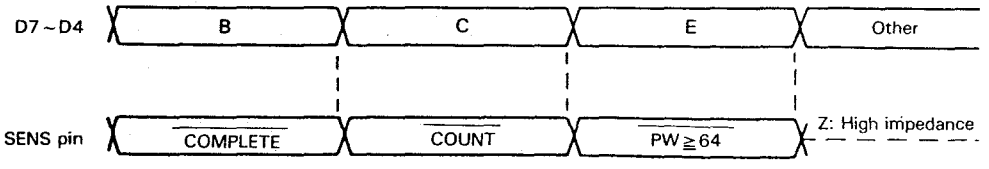


Fig. 3 Timing chart of SENS pin

CIRCUIT DESCRIPTION

(5) Sub code output

Sub codes P ~ W loaded in the 8-bit shift register are output out of SBSO pin in accordance with the clock input through EXCK pin. When SCOR pin is "H", S0 + S1 signal is output. Sub code Q is as follows, depending on the SQEX pin status.

a. When the SQEX pin is "L", sub code Q is output from the SUBQ pin in synchronism with the WFCK signal in the same way as for the CX23035. The $\overline{\text{WFCK}}$ is also output from the SQCK pin.

b. When the SQEX pin is "H", sub code Q is output from the SUBQ pin in synchronism with the external clock (as from the microprocessor). Two 80-bit shift registers, for reading and writing, are incorporated as shown in Fig. 7, and while the microprocessor reads, the new sub code Q is written to another register. The microprocessor is interrupted from the outside at the rising edge of the SCOR pin, and after checking the CRCF flag (output to the CRCF pin, or the SUBQ pin when the CRCQ flag is "1"), the CRCF is checked. If CRCF = "H", a shift lock is output and the new sub code Q is read. After the LSB side is replaced with the MSB side by a unit of 4-bit, the data is stored in register. As the microprocessor serially inputs from the LSB first, replacing the 4-bit of data is unnecessary.

(a) Timing of SBSO, SUBQ, SCOR, CRCF

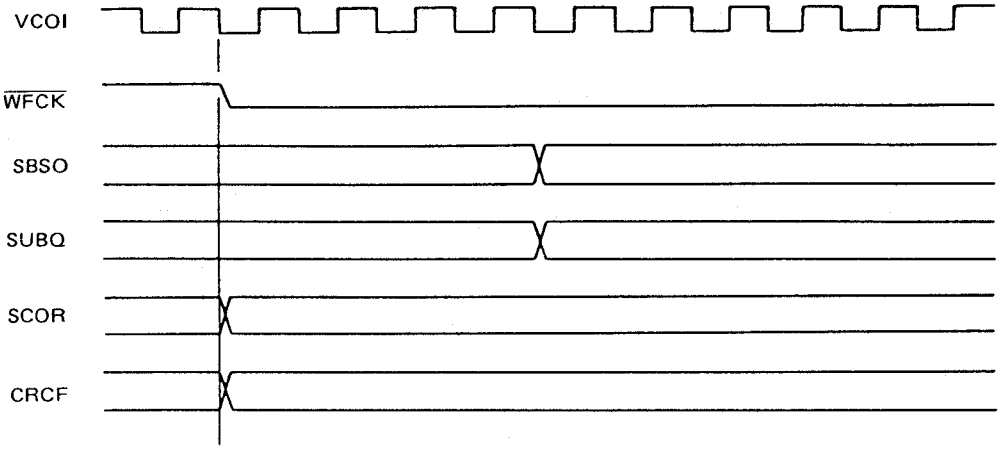
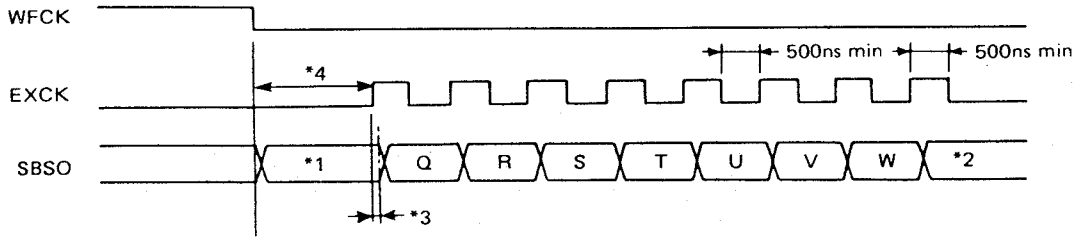


Fig. 4

(b) Timing of SBSO, EXCK



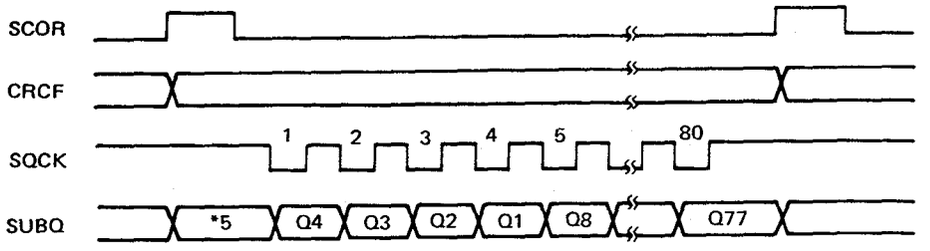
*1: Sub code P is output when SCOR is 0.
S0 + S1 is output when SCOR is 1.
*2: SBSO is 0 when 8 or more pulses are input to EXCK.
*3: 4T ~ 6T if the period of VCO is expressed as T.
*4: Make EXCK low for 10 μs from the rising edge of WFCK.
One time period of T = 8.6436 MHz.

Fig. 5 Timing chart of sub code outputs

CIRCUIT DESCRIPTION

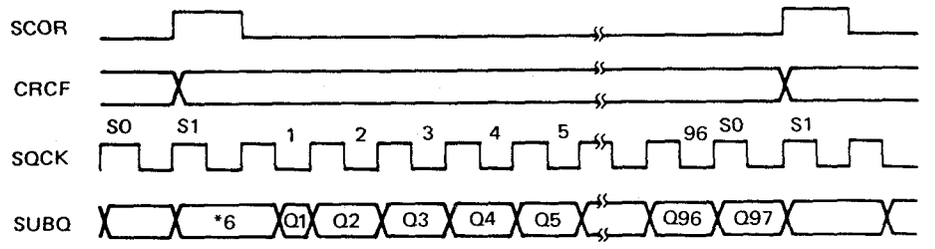
(c) Timing of SCOR, CRCF, SQCK, SUBQ

SQEX = "H" level



*5:CRCF when CRCQ flag is "1", undefined when "0".

SQEX = "L" level



*6:CRCF when CRCQ flag is "1", Q98, Q1 when "0".

Fig. 6 Timing chart of sub code outputs

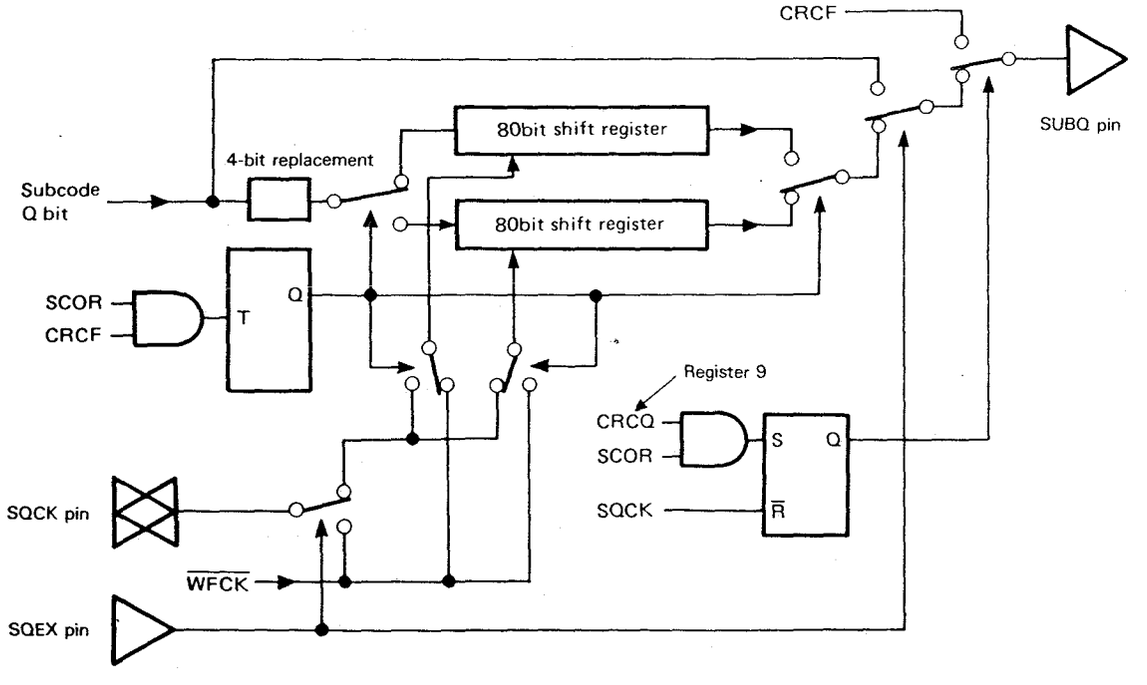


Fig. 7

CIRCUIT DESCRIPTION

2. EFM demodulation

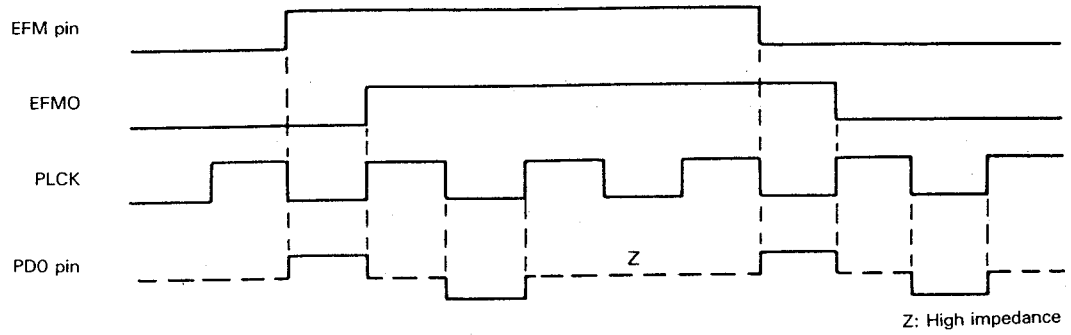
(1) Playback of bit clock by EFM-PLL circuit

The EFM signal read out of the optical block contains a clock component of 2.16 MHz. Therefore, it is possible to take out a bit clock (PLCK) of 4.32 MHz synchronized with this clock by the EFM-PLL circuit.

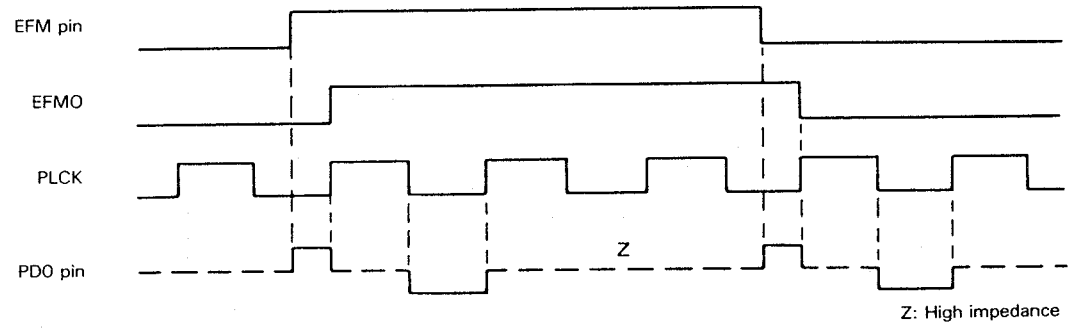
At each edge of EFM signal, phase comparison is made with PLCK, which is 1/2 of VCO, is made and output is made by TRI STATE out of PDO pin. The mean value of PDO pin is about 1/2 VDD if synchronized, but the mean value drops when VCO becomes higher. On the other hand, the mean value increases when VCO becomes less.

The timing charts of EFM pin, EFMO, PLCK and PDO are shown in Fig. 8.

(a) When EFM signal and VCO are synchronized



(b) When VCO is higher than EFM signal



(c) When VCO is less than EFM signal

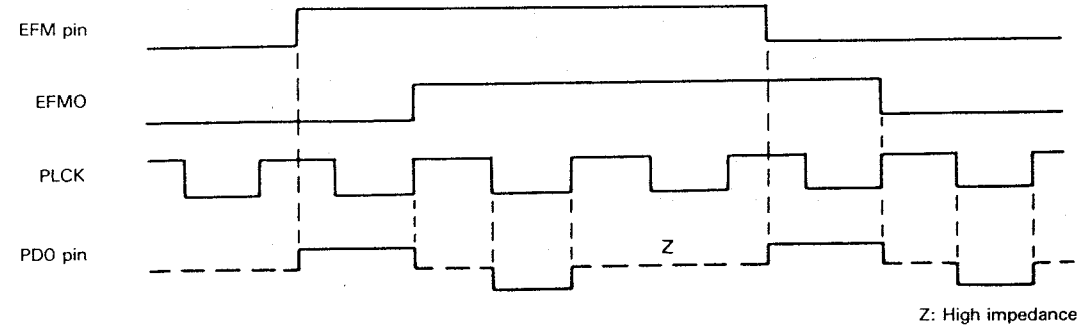


Fig. 8 Timing charts of EFM-PLL circuit

CIRCUIT DESCRIPTION

(2) Detection, protection and interpolation of frame synchronizing signals

There are cases during recording where the same pattern is detected in the data due to the influence of drop-out and jitter, even if a pattern that is same as the synchronizing signal will not appear.

On the other hand, there also are cases where original frame synchronizing signal is not detected. Therefore, protection and interpolation are required besides detection.

The edge portion only of EFM signal (EFMO) latched with PLCK is converted to "1" and the rest to "0", and then input is to a 23-bit shift register and a frame synchronizing signal is detected.

In order to protect a frame synchronizing signal, a window is provided and the same patterns outside of this window are removed. This width can be selected with WSEL.

If no frame synchronizing signal is located in this window, interpolation is made with a signal produced by 588-mal counter (4.3218 MHz/588 = 7.35 kHz)

A 4-bit counter for counting the number of these frames to be interpolated is provided, and when its count reaches the level selected with GSEL, GSEM, the window is ignored and the 4-bit counter is reset with the next frame synchronizing signal. The GTOP pin is of "H" while this operation is performed. Further, GSF pin is of "H" when the frame synchronizing signal generated by the 588-mal counter for making interpolation is synchronized with the frame synchronizing signal from the disc.

The frame synchronizing signal before passage through the window or the window is output out of UGFS (DA05 pin at the time when PSSL = L).

WSEL	Window width
0	±3 clock
1	±7 clock

GSEM	GSEL	Number of frame to be interpolated	UGFS (PSSL = L)
0	0	2 frames	Window
0	1	4 frames	Window
1	0	8 frames	Frame synchronizing signal before passage through window.
1	1	13 frames	Window

The timing for write request signal (WREQ). Write Frame Clock (WFCK), etc. is generated based on the protected and interpolated frame synchronizing signal.

(3) EFM demodulation

14-bit data is taken out of the 23-bit shift register and is demodulated to 8-bit data through 14 ➔ 8 conversion circuit composed of array logics. Then a write request (WREQ) signal is output to the RAM interface block, and the data is then output to the data bus (DB08 - DB01 pins) of the RAM in accordance with the OENB signal transmitted from said block.

3. Sub code demodulation

(1) Sub code demodulation

Synchronizing signals S0 and S1 of 14-bit sub codes are detected out of the 23-bit shift register, and sampling is made in the timing that is synchronized with WFCK.

After delay of S0 by one frame, S0 + S1 is output out of SCOR pin and S0 · S1 is output out of SBSO pin (only when SCOR = H).

Data (P - W) of sub codes only is input to the register in the timing synchronized with WFCK after EFM demodulation; and sub code Q is output out of SUBQ pin, and at the same time, it is loaded in the 8-bit shift register and is output out of SBSO pin in correspondence to a clock from EXCK pin.

The details of this timing will be shown in **"1, CPU interface"**. (Page 26)

(2) Sub code Q error detection

The CRC result of sub code Q is output from the CRCF pin in synchronism with the SCOR pin.

It goes "L" when an error is detected. If the CRCQ flag is "1" at this time, the CRCF flag is output from the SUBQ pin during the time from the rising edge of the SCOR pin to the trailing edge of the SUBQ pin. This timing is detailed in **"1. CPU interface"**.

CIRCUIT DESCRIPTION

4. RAM interface (generation of external RAM address)

(1) Request from EFM demodulation block (Write RAM request)

When one symbol of demodulation is complete in the EFM demodulation block requests to write data to the external RAM to the RAM interface block. This request is WREQ signal.

This block gives priority orders to requests from other blocks and processes these requests.

When EFM write request is received, an address is generated to the RAM and Write Enable state is produced. Furthermore, a data output instruction is issued against the EFM demodulation block. This instruction is OENB signal.

Clocks of PLL system are used for EFM block and for requests (WREQ) from EFM block, but clocks of X'tal system are used for processing thereafter.

(2) Request from D/A converter output circuit (Read to D/A request)

This is a de-interleaved data request issued out of the timing generator in this block.

This request is of the highest priority among all requests, and addresses of three types are generated against this request.

This request is generated once every 24 periods based on the period of system clock **C212 (8.4672 MHz/4)**. The data output out of the RAM is C2 pointer first, less significant 8-bit out of 16-bit and finally more significant 8-bit.

(3) Request from error correction block (C1/C2 correction, pointer R/W)

The error correction block requests the data located on the system (C1/C2) to be corrected. Furthermore, there is a request to rewrite incorrect data to correct data.

In addition, there is a request for pointer R/W which indicates reliability of data.

These requests are made by the 8-bit data directed to the RAM interface block from the error correction block.

The requests from the error correction unit are of the lowest priority among requests of three types.

After acceptance of a request, data from RAM is directed to the 3rd clock of C212.

The data of acceptance of a request is output to the error correction block as a PREN signal.

This block generates type address of the requested data, and controls R/W of the RAM at the same time.

(4) Address generation

The data after EFM demodulation is data subjected to interleave processing.

This interleave processing is subjected to data lag by the unit of a frame.

Data of 108 frames are required for de-interleave. In other words, for obtaining one frame of audio data played in a certain length of time, data of 108 frames after EFM demodulation are required. Further, the system data of C1/C2 is of the system in the process of application of interleave, and therefore, is included in 108 frames.

Data in practice are generated continuously. That is, de-interleave should be updated by the unit of a frame. Therefore, Read/Write base counters are required. This base counter performs counting by the unit of a frame.

The writer base counter is used only at the time of EFM data writer.

The address directed to the external RAM is determined by the relative lag value to EFM demodulation data and their number of frames.

(5) Priority of address generation request

The system control block determines priority of address generation requests made to the RAM interface block.

The priority order is as follows, beginning with higher priority.

1. Read to D/A request
2. Write to RAM request
3. C1/C2 request

The number of times of requests is as follows.

1. Requests of 12 times in the frame section
   The number of times of address generation to it is 36 times.
2. Requests of 32 times in the frame section
   The number of times of address generation to it is 32 times.
3. Maximum number of times of request (C1 Double error correction, C2 pointer copy)
   Read R/W 64 times, Point R/W 65 times in one frame section
   The number of times of address generation to it is 129 times.

CIRCUIT DESCRIPTION

288 C212 (clocks) are included in a frame, and the number of times of operation of the RAM in it is 197 times at maximum.
In the system control block, against request 1, the timing of its occurrence is reserved in advance. Requests 2, 3 are generated simultaneously, priority is given to request 2, and if a request is generated during execution of either request, priority is given to the job in execution.

(6) Jitter margin

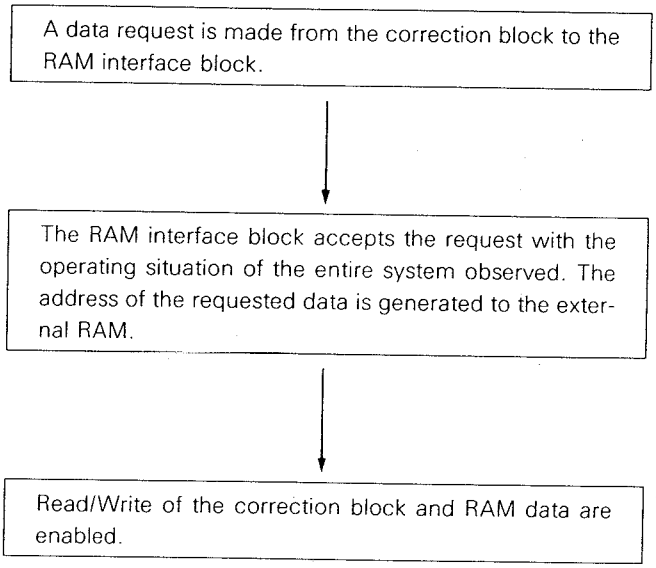
The EFM demodulation data is synchronized with data's playback system (PLL) as described earlier. Accordingly, it includes disturbance (wow, flutter, etc.) of disc rotation servo, etc. It is loaded to the external RAM. As the data taken out of the RAM is synchronized with the clock of X'tal system, this RAM is subjected to time axis correction.
However, the limit of time axis correction is determined by the capacity of the RAM. In this system, other data is destroyed when read/write frames are spaced apart by ±5 frames. In such a status how the playback sound is cannot be guaranteed. The base counter monitor is provided in order to avoid it.
In other words, when the difference between read base counter and write base counter exceeds ±4 frames, the write base counter is set in the value of the read base counter.
As a result, there is no case where data without error correction is output to the D/A.
The RAOV signal is of "H" for one frame (WFCK) section when the difference between base counters exceeded ±4 frames.

5. Error correction

(1) The error correction block makes correction up to double errors with each of C1 correction and C2 correction.
(2) This system adopts a unique pointer erasure method in order to minimize erroneous correction. Accordingly, the external 16K RAM stores these pointer data in addition to audio data.
(3) The pointer generated in C1 correction is called C1 pointer and the pointer generated in C2 correction is called C2 pointer.
(4) When the data of C1 system is judged as reliable, a C1 pointer is set in this system.
(5) During C2 correction, whether correction is to be made or not to be made and whether the data is reliable or unreliable are judged from the error location, locations and number of C1 pointers obtained through computation. A C2 pointer is set against an unreliable word (16-bit).
(6) The word in which a C2 pointer was set is subjected to previous value hold or mean value interpolation when it is output out of this LSI.
(7) Terminal C2FL becomes "H" when one or more C1 pointers are set in the data included in the C2 system at the time of C2 correction. C2FL is reset to "L" in minimum 472ns (see Note) after deactivation of pin RFCK. C2FL is the AND of C2F1 and C2F2.

Note: 472ns: One period of 2.1168 MHz

(8) The flow of data with the external RAM is as follows.


A data request is made from the correction block to the RAM interface block.
The RAM interface block accepts the request with the operating situation of the entire system observed. The address of the requested data is generated to the external RAM.
Read/Write of the correction block and RAM data are enabled.

(9) When PSSL is set at "L", a signal that is capable of monitoring error correction is output.
C1F1, C1F2, C2F1 and C2F2 output to DA01 - DA04 are these monitor signals. These signals are reset to "L" when a period of minimum 472ns has elapsed since deactivation of RFCK.
The levels and meanings of these signals at the time of deactivation of RFCK are as follows.

CIRCUIT DESCRIPTION

C1F1	C1F2	C1 correction status
0	0	No error
1	0	Single error correction
0	1	Double error correction
1	1	Irretrievable error

C2F1	C2F2	C2FL	C2 correction status
0	0	0	No error
1	0	0	Single error correction
0	1	0	Double error correction
1	1	1	Irretrievable error

6. CLV servo control

The spindle motor revolution is controlled with one selected out of the following seven modes in accordance with a command from the CPU. CLV is the abbreviation of Constant Linear Velocity. The output is composed of MDP pin for controlling synchronization of velocity and phase, MDS pin for controlling synchronization of velocity, FSW pin for making selection of filter constant and MON pin for controlling motor ON/OFF.

(1) STOP: Register E = 0000'B (B means binary)
Mode for stopping the spindle motor.
MDP = FSW = MON = "L", MDS = "Z"

(2) KICK: Register E = 1000'B
Mode for running the spindle motor in forward direction.
MDP = MON = "H", MDS = "Z", FSW = "L".

(3) BRAKE: Register E = 1010'B
Mode for running the spindle motor in reverse direction.
MDP = FSW = "L", MDS = "Z", MON = "H".

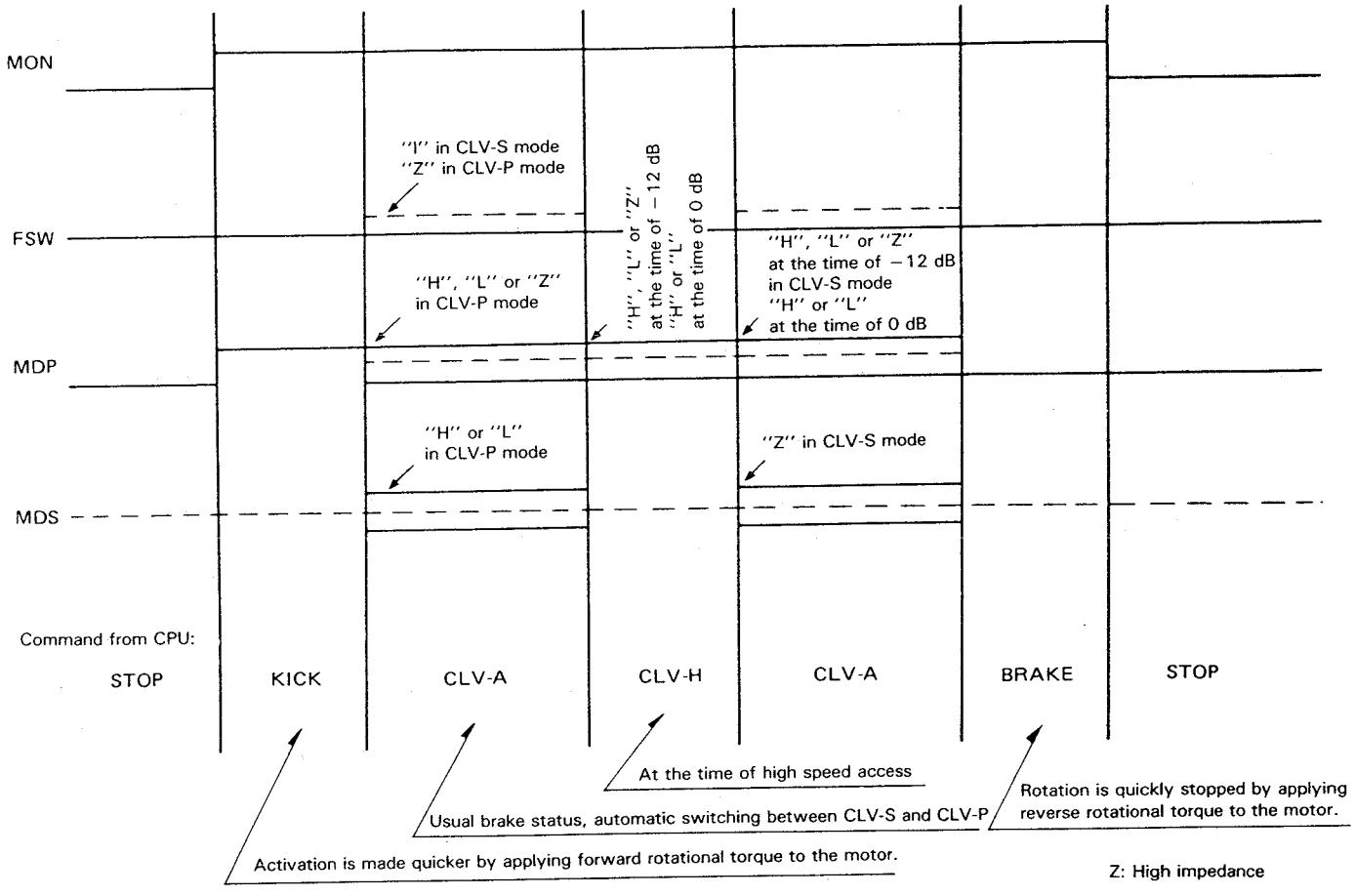


Fig. 9 Typical control of spindle motor

CIRCUIT DESCRIPTION

(4) CLV-S: Register E = 1110'B

Rough servo mode used at the time of start of rotation, at the time of track jump and also when the EFM-PLL circuit is unlocked due to another reason.

When the period of VCO's oscillation frequency 8.6436 MHz is expressed as "T", the pulse width of a frame synchronizing signal is "22T" during specified revolution, and it is the maximum pulse width in a period of RFCK. In practice, however, there are pulses having widths over "22T" due to drop-off of EFM signal due to other reasons, and the frame synchronizing signal cannot be correctly detected unless such pulse are removed. Therefore, the maximum value (peak) of the pulse width of EFM signal is detected (called peak hold) in the period of RFCK/2 or RFCK/4, than the minimum value in this peak is detected (called bottom hold) in the period of RFCK/16 or RFCK/32, and this value is used as the frame synchronizing signal.

"L" is produced out of MDP pin while the frame synchronizing signal is "21T" or less, "Z" when it is "22T", or "H" when it is "23T" or more. Either 0 dB or 12 dB can be selected as its gain.

MDS = "Z", FSW = "L", MON = "H".

(5) CLV-H: Register E = 1100'B

Rough servo mode used at the time of high-speed access.

Assuming there are 20,000 tracks, from the innermost to the outermost, and that this distance is accessed in 1 second, the mirrors (portions where there are no pits) between tracks result in a 20 kHz signal, which is superimposed on the EFM signal. When such a signal is input in the CLV-S mode, a longer mirror section than the actual frame sync signal is detected as the peak value, resulting in an unstable servo.

Therefore, in order to stabilize the servo during high-speed access, the CLV-H mode performs the peak hold at a period of 8.4672/256 MHz (about 34 kHz). Then, like the CLV-S mode, it performs the bottom hold at a period of RFCK/16 or RFCK/32. Except for the period of peak detection, other operations of the CLV-H mode are the same as for the CLV-S mode.

Pwmdx: Pulse width after bottom hold
TB: Bottom hold period, i.e. RFCK/16 or RFCK/32
Z: High impedance

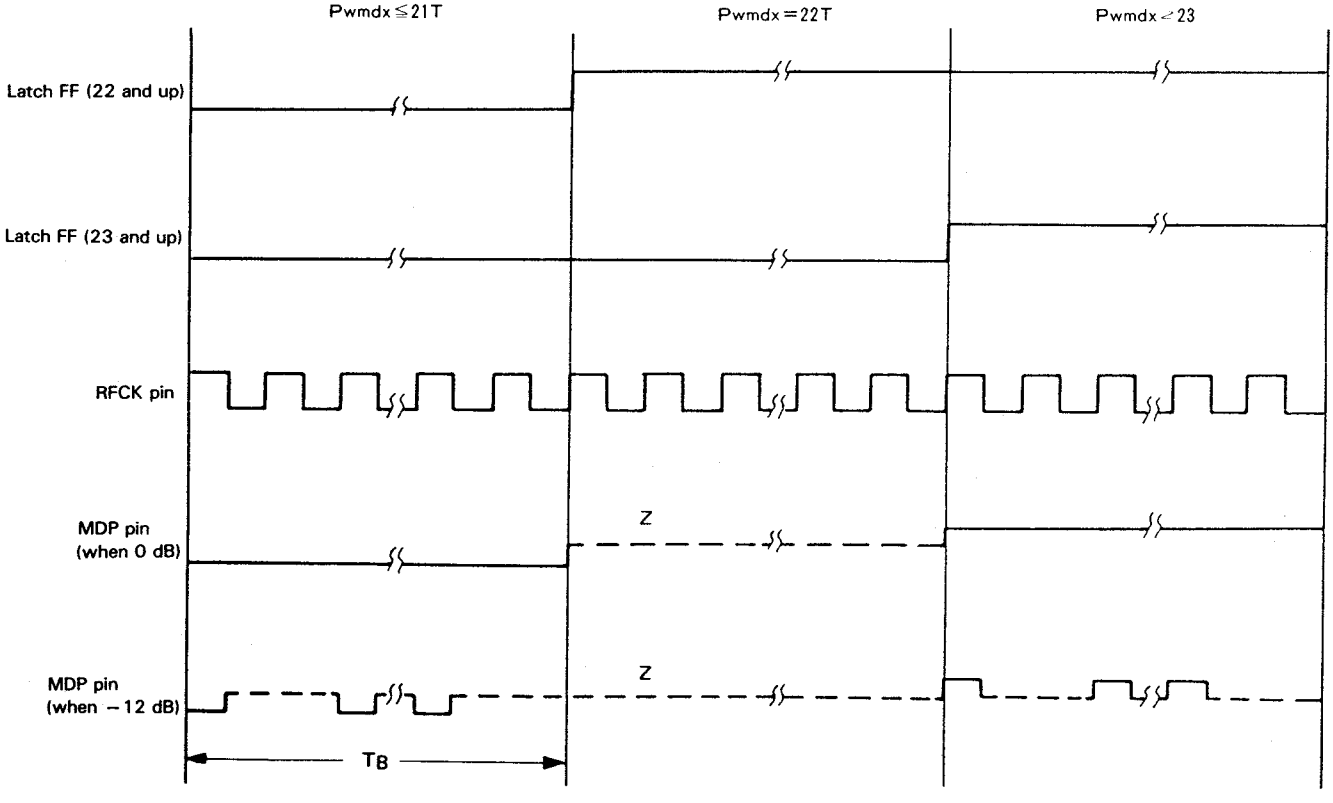


Fig. 10 Timing chart in CLV-S, CLV-H mode (1)

CIRCUIT DESCRIPTION

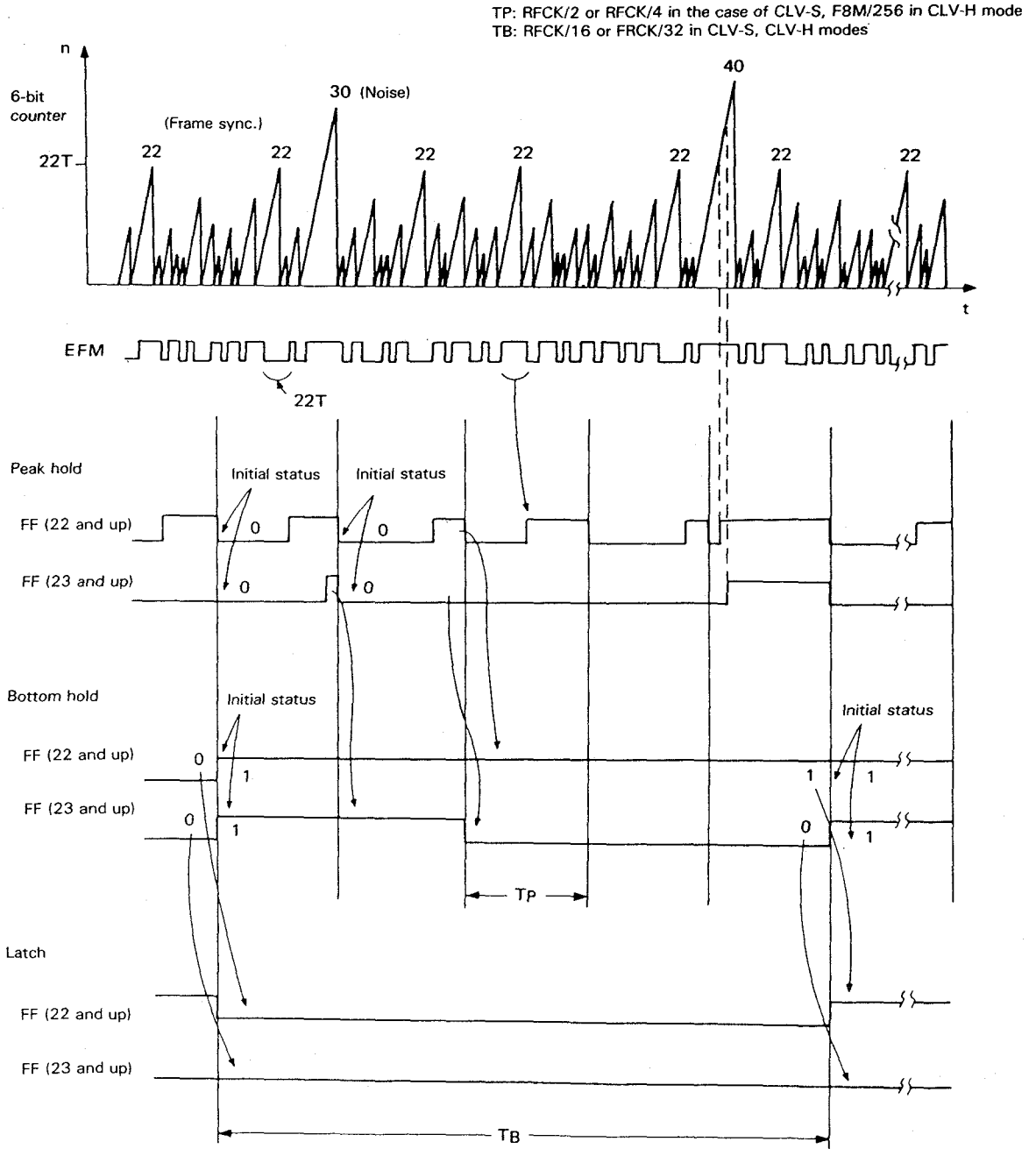
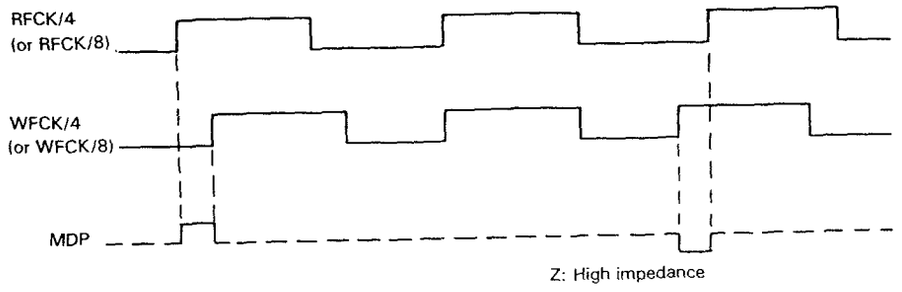


Fig. 11 Timing chart in CLV-S, CLV-H mode (2)

CIRCUIT DESCRIPTION

(6) CLV-P: Register E = 1111'B
PLL servo mode.
When the NCLV of register 9 is "0", the phase of the WFCK/4 signal and the phase of the RFCK/4 signal are compared and output to the MDP pin. When NCLV = "1", 1/4 of the base counter frame frequencies at the Write side and the Read side are phase-compared and output to the MDP pin. It goes "H" when WFCK is slow, "L" when it is fast, and is "Z" when synchronized.
Assuming the 8.4672/2 MHz period is T, and the time when WFCK is "H" is thw, the MDS pin outputs a signal which goes "H" during the time from the trailing edge of WFCK to the time represented by (thw-279T) × 32, and then goes "L" until the next trailing edge of WFCK.
MDS = "H" when thw ≧ 279T,
MDS = "L" when thw ≦ 279T.
The MDS pin varies between 32T and 544T, in 32T steps, when 280T ≦ thw ≦ 296T. For example, when synchronized (rotating at the standard speed), that is when thw = 288T, a 7.35 kHz signal, with a duty cycle of 50% is output.
FSW = "Z", MON = "H".

MDP pin



5) MDS pin (The period of 4.2336 MHz is expressed as "T".)

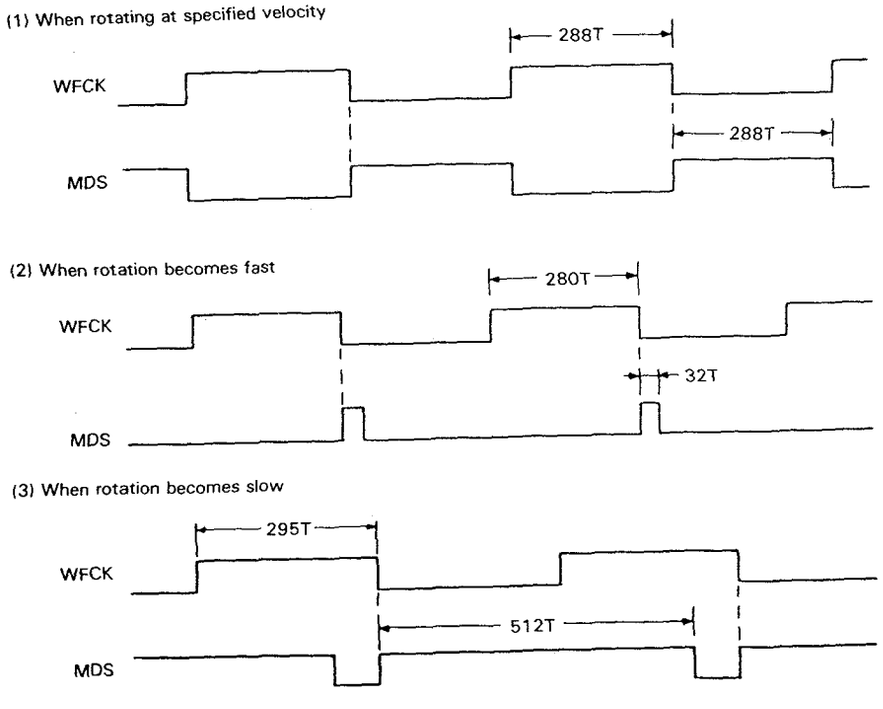


Fig. 12 Timing chart in CLV-P mode

CIRCUIT DESCRIPTION

(7) CLV-A: Register E = 0110'B

The mode used for normal play status.

The GFS signal (''H'' when locked, ''L'' when unlocked), after frame sync detection, protection and interpolation block, is sampled at WFCK/16, and functions in CLV-P mode when the signal is ''H''. When the ''L'' signal continues for 8 times, the mode is automatically changed to CLV-S mode.

When in the CLV-S mode, setting of the peak hold period, and setting of the period and gain of the bottom hold of the CLV-S and CLV-H are performed in register D, and the selection of each mode is performed in register E. The description of these registers are detailed in **''1. CPU interface''**. (Page 26)

Note:

When PSSL = ''L'', DA07 pin outputs WFCK/4 or WFCK/8 as FCKV, and DA08 outputs EFCK/4 or EFCK/8 as FCKX.

(8) CLV-A': Register E = 0101'B

New auto servo mode added to the CX23035.

The difference between CLV-A' and CLV-A is in the rough servo system. With the old rough servo system, the EFM pattern is measured by a crystal and the servo is applied so that the width of the sync pattern is a fixed value, and the rotation speed of the spindle motor is roughly fixed. In this case, if the value is out of the VCO capture range, the VCO never locks with the EFM. With the new rough servo system, a VCO is used for measurement instead of a crystal. If the VCO center is shifted from true center the VCO tends to lock, since the rotation of the spindle motor varies in the same direction.

The new rough servo functions only in CLV-A' mode. The rough servo in CLV-A mode and CLV-S mode is the old rough servo.

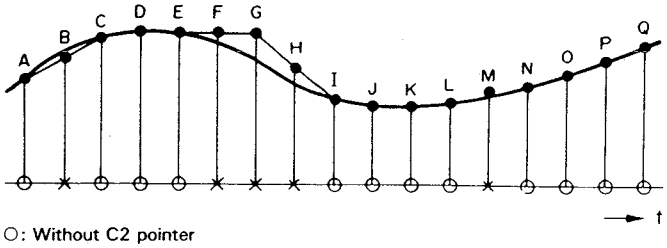
CIRCUIT DESCRIPTION

7. Interpolation and mute, attenuate

(1) Interpolation circuit block

3-byte data can be obtained with a Read to D/A request. They are C2 pointer, less significant 8-bit and motor significant 8-bit. The total 16-bit constitute the data generated per sampling (2's complement.)

The C2 pointer expresses the reliability of this 16-bit data. Therefore, data with C2 pointer is subject to interpolation in this block.



O: Without C2 pointer
X : With C2 pointer

Fig. 13

Mean value interpolation

$$B = \frac{1}{2}(A + C)$$

$$H = \frac{1}{2}(E + I)$$: When pointers are continuous

$$M = \frac{1}{2}(L + N)$$

Previous value hold

$$F = G = E$$

16-bit data is alternately output to L-ch and R-ch, R-ch data is output in the section in which LRCK is "L" and L-ch data is output in the section in which LRCK is "H".

C2PO signal outputs C2 pointer to the 16-bit data directed DA01 - DA16 (PSSL = H), DA16 (PSSL = L).

In other words, it means that the 16-bit data that is output when C2PO is "H", is interpolated data.

(2) Explanation of muting and attenuator

In the muting block it is possible to mute ($-\infty$ dB) or attenuate (-12 dB) the audio signal in accordance with the MUTG pin and ATTM signal of the CPU interface block.

When the ZCMT flag of register 9 is "1", the input from the MUTG pin is valid only if all of the audio data higher 6-bit (including the sign bit) are "1" or "0".

Note that switching the MUTG pin does not cause muting if the data zero-cross does not occur. To eliminate this problem, after switching the MUTG pin "H" or "L" with ZCMT = "1", ZCMT shall be turned "0" in a specified period of time, regardless of whether the zero-cross causes muting ON/OFF or not.

ATTM	MUTG	Attenuation value	Remarks
0	0	0 dB	
1	0	−12 dB	
0	1	$-\infty$ dB	(See Note)
1	1	−12 dB	(See Note)

Note:
When the MUTG is set to "H" level with the NCLV flag set to "0", the read base counter value is continuously loaded into the write base counter as well as the muting.
Except at CLV-A, CLV-P, CLV-S, or CLV-A' with the NCLV flag set to "1", the base counter value is loaded.

CIRCUIT DESCRIPTION

8. Mode setting

The various kinds of mode can be set by combining the following pins. (Refer to Table 2.)

MD1 pin : Mainly for selection of the oscillator clock at the XTAI or XTAO pin.
MD2 pin : Mainly for selection of the digital out function.
MD3 pin : Mainly for selection of the digital filter function.
PSSL pin : Mainly for selection between serial and parallel output.
SLOB pin : Selection between offset binary and 2's complement.

Input pin					Function					(Note)	Compatible IC	
MD1	MD2	MD3	PSSL	SLOB	8M/16M	DO OFF/ON	DF OFF/ON	P/S	OB/2's	CD ROM/AUDIO	CXD1125	CXD1130
L	L	L	L	L	16M	DO ON	DF ON	Seri	2's	AUDIO		
L	L	L	H	H	↓	↓	↓	Para	OB	↓		
L	L	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	
L	H	L	L	L	↓	DO OFF	DF ON	↓	↓	↓		○
L	H	L	H	H	↓	↓	↓	Para	OB	↓		○
L	H	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	○
L	H	H	H	H	↓	↓	↓	Para	OB	↓	○	○
H	L	L	L	L	8M	↓	DF ON	Seri	2's	↓		○
H	L	L	H	H	↓	↓	↓	Para	OB	↓		○
H	L	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	○
H	L	H	H	H	↓	↓	↓	Para	OB	↓	○	○
H	H	H	L	L	16M	DO ON	↓	Seri	2's	CD ROM	○	
H	H	H	H	L	8M	DO OFF	↓	↓	↓	↓	○	○

Note:
- **8M/16M: Selection of clock, XTAI or XTAO. 8.4672 MHz/ 16.9344 MHz**
- **DO OFF/ON: Digital out OFF/ON**
- **DF OFF/ON: Digital filter OFF/ON**
- **P/S: Parallel output/serial output**
- **OB/2's: Offset binary/2's complement**
- **CD ROM/AUDIO: Compatible to CD ROM/Compatible to audio**

Table 2

- **Selection of clock**

The oscillator clock for XTAI and XTAO is available at 16.9344 MHz and 8.4672 MHz. However, when digital output is used, the clock must be set to 16.9344 MHz.

- **Selection of digital filter (Refer to "9. Digital filter".)**

When the digital filter function is set to ON, the DAC interface signal are all set to double speed.

- **Selection of parallel output/serial output**

When the parallel output is selected, DA01 to DA16 pins output the 16-bit parallel data.

When the serial output is selected, DA01 to DA16 pin output the following signals respectively.

C1F1 (DA01) :
C1F2 (DA02) : Error correction status monitor output at C1 decode.
C2F1 (DA03) :
C2F2 (DA04) : Error correction status monitor output at C2 decode.
C2FL (DA05) : Correction status output, C2FL = C2F1·C2F2.
C2PO (DA06) : C2 pointer signal.
RFCK (DA07) : Read frame clock signal, 7.35 kHz when locked to the crystal line.
WFCK (DA08) : Write frame clock signal, 7.35 kHz when locked.
$\overline{\text{PLCK}}$ (DA09) : 1/2 of the divided signal from the VCO pin, 4.3218 MHz when locked.
UGFS (DA10) : Non-protected frame sync signal.
GTOP (DA11) : Frame sync protect status display signal.
RAOV (DA12) : Jitter margin over or underflow display signal.
C4LR (DA13) : 4 times the LRCK signal.
$\overline{\text{C210}}$ (DA14) : Bit clock (invert signal of C210).
C210 (DA15) : Internal system clock (4.2336 MHz when DF is ON, 2.1168 MHz when CXD1125Q or DF is OFF).
DATA (DA16) : Serial data output (MSB or LSB first output).

CIRCUIT DESCRIPTION

• Selection of offset binary/2's complement

When the SLOB pin is "H", an offset binary signal is output, and when it is "L", a 2's complement signal is output.

• Selection of CD ROM/audio compatibility

When MD1 = MD3 = "H", the player is compatible with a CD ROM and outputs the C2 pointer for each byte. At the same time, the average value interpolation and the previous value holding operations are not performed. For example, when there is an error in the upper 8-bit of the 16-bit, only the C2 pointer corresponding to the upper 8-bit goes "H", and the lower 8-bit are processed as the correct data.

9. Digital filter

The built-in digital filter has the following features:

1. Correction of the aperture effect
2. Small attenuation at 20 kHz
3. Practical-design filtering band ranges

(1) Filter characteristics

Passing Band	Ripple from DC to 18 kHz	±0.07 dB max.
	Attenuation of 20 kHz with respect to 1 kHz	0.65 dB max.
Filtering Band	Attenuation of 44.1 ± 1 kHz with respect to 1 kHz	87 dB min.
	Attenuation of 44.1 ± 5 kHz with respect to 1 kHz	58 dB min.
	Attenuation of 44.1 ± 10 kHz with respect to 1 kHz	44 dB min.
	Attenuation of 44.1 ± 20 kHz with respect to 1 kHz	10 dB min.
	Frequency range in which attenuation is −30 dB with respect to 1 kHz	44.1 ± 14 kHz
	Frequency range in which attenuation is −60 dB with respect to 1 kHz	44.1 ± 4 kHz

10. Countermeasures to defect

To counter a defect, the PDO pin is set to "Hi-Z" during the time until GFS goes "H" again after inverting from "H" to "L" or after about 0.55 ms has elapsed. However, this operation is performed only when the HZPD flag of register 9 is "1". When HZPD = "0", it will never be set to "Hi-Z".

The signal switching between the rough servo in the CLV-A or CLV-A' mode and the PLL servo is output from the LOCK Pin.

After the GFS signal is sampled at WFCK/16, and when the signal is "1", the LOCK pin goes "H", when a "0" is present 8 times in a row, the LOCK pin goes "L".

This operation is similar to that for the FSW pin.

However, while the FSW outputs a fixed signal when not in CLV-A or CLV-A' mode, the LOCK pin always output the above signal.

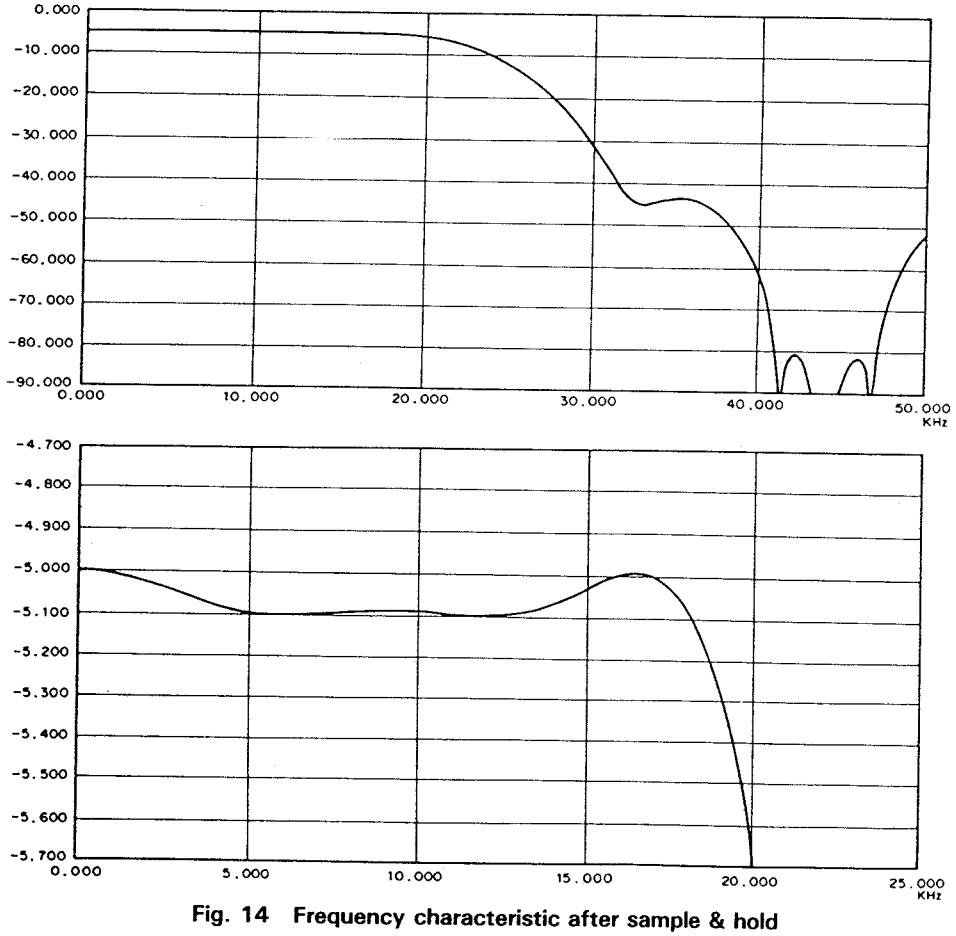
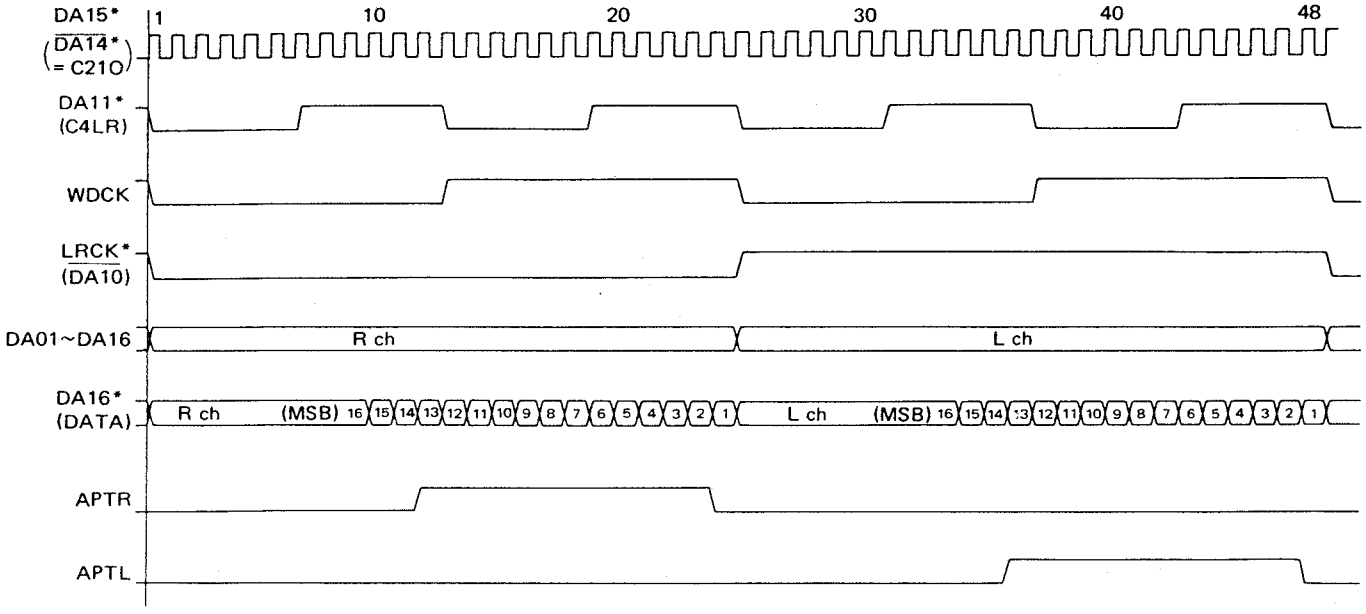


Fig. 14 Frequency characteristic after sample & hold

CIRCUIT DESCRIPTION

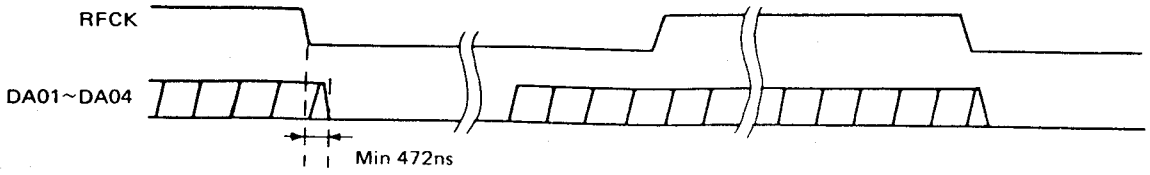
- **Timing chart**



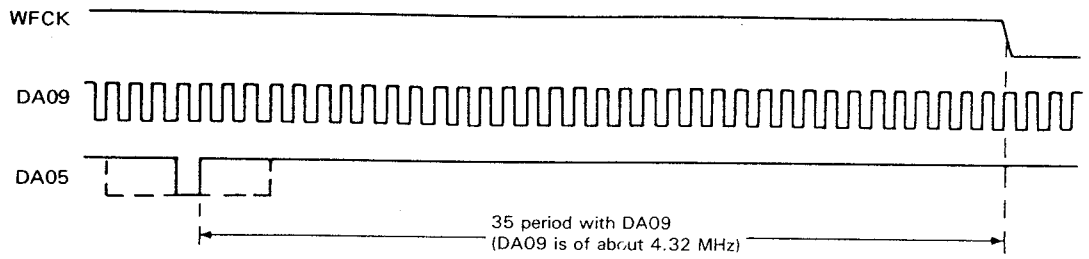
* When PSSL = "L".

Fig. 15 Timing chart of audio output

CIRCUIT DESCRIPTION



* DA01 to DA04 (C1F1, C1F2, C2F1, C2F2) are cleared when a period of minimum 472 ns has elapsed since RFCK was deactivated.
* AND signal of C2F1 and C2F2 is output out of C2FL pin.



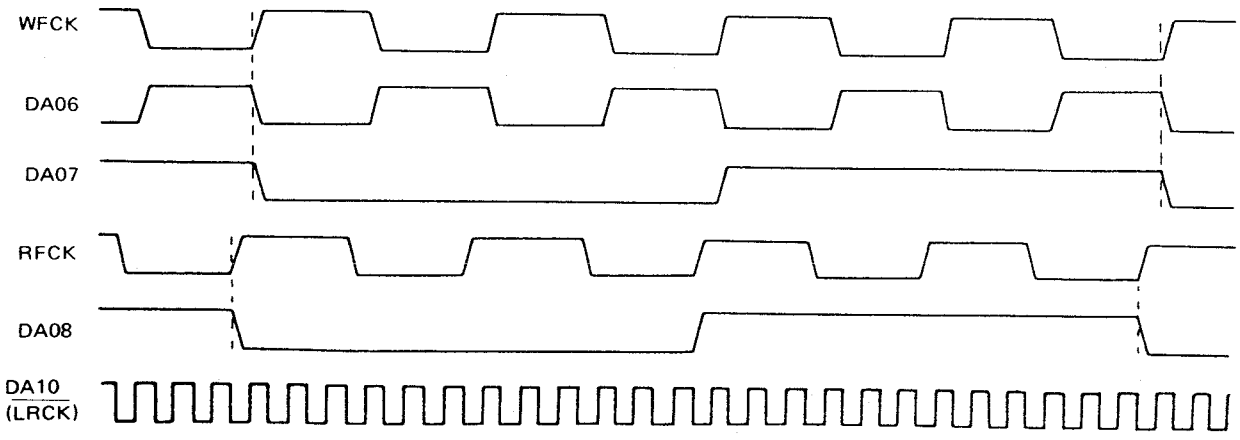


Fig. 16 Timing chart of DA01 to DA16 output when PSSL = "L"

CIRCUIT DESCRIPTION

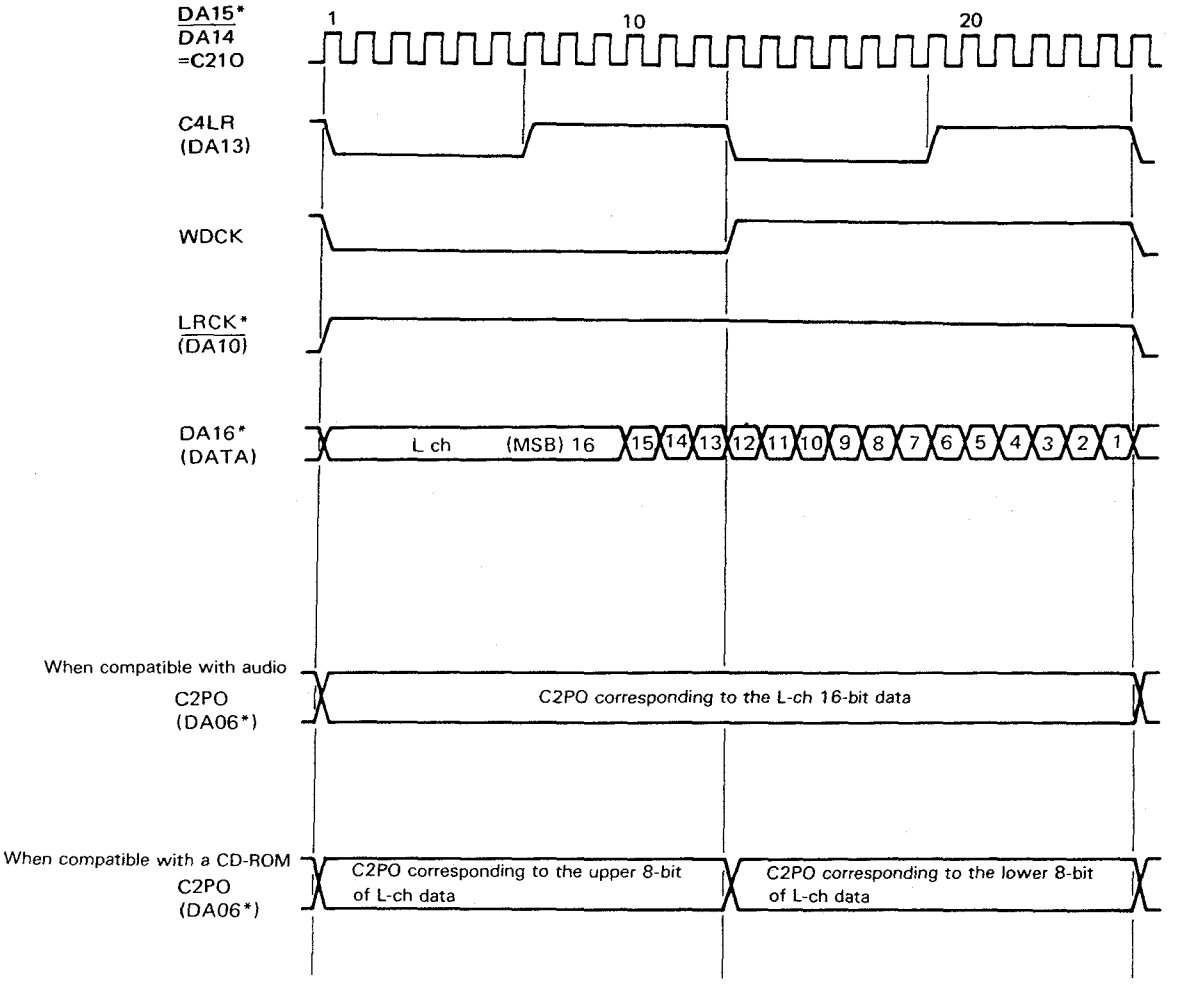


Fig. 17 Timing chart of C2PO output (when PSSL = "L")

* RAOV becomes "H" for one frame (synchronized with WFCK) when a jitter that exceeds ±4 frames is generated between RFCK and WFCK.

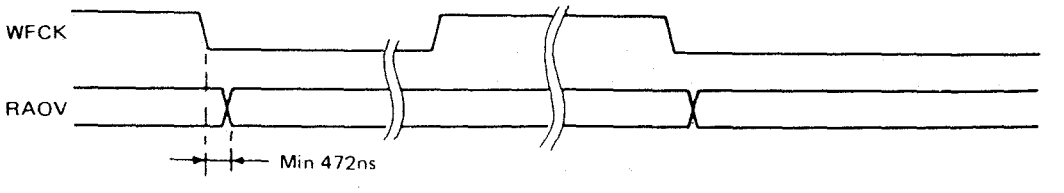


Fig. 18 Timing chart of RAOV output

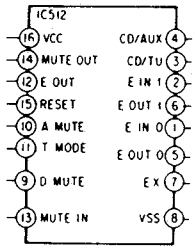
CIRCUIT DESCRIPTION

Master microcomputer, mechanism microcomputer and I/O control microcomputer

This unit has three microcomputers. A master microcomputer (IC506), a mechanism control microcomputer (IC505) and an I/O control microcomputer (IC512).

IC512: MB88201 I/O control microcomputer

The I/O control microcomputer is used for mutual control with externally connected components and for synchronizing the muting timing.



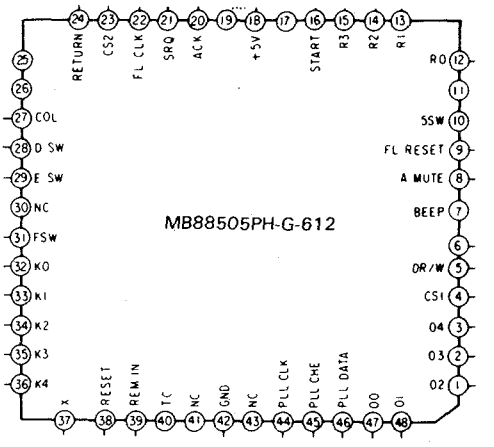
IC512: I/O control microcomputer

Initial (Initial Status)	Pin No.	Pin Name	I/O	Functionse	Pin No. 3 CD/TU	4 CD/AUX	5 EOUT 0	6 EOUT 1	14 MUTE OUT	ACTIVE
H	1	E IN 0	I	Accepts operations from external components (output side)	H	L	L	H	L	L
H	2	E IN 1	I	Accepts operations from external components (input side)	H	L	H	L	H	L
H	3	CD/$\overline{TU}$	O	Select switch to alternate between CD (or external input) and tuner (TU)						High when CD is selected
H	4	CD/$\overline{AUX}$	O	Select switch to alternate between CD and AUX (external input). Also for remote output to system components (detected at rising time)						High when CD is selected
L	5	EOUT 0	O	Remote output to external component (output side)						H
L	6	EOUT 1	O	Remote output to external component (input side)						H
—	7	EX	—	Oscillator, about 1 MHz						
OV	8	Vss	—	GND						
H	9	DMUTE	I	Accepts the digital mute signal from the mechanism controller (effective only when CD is engaged)	—	—	—	—	L	H
H	10	AMUTE	I	Accepts an analog mute signal from a system component	—	—	—	—	L	H
H	11	T MODE	I	Accepts operations from a tuner (valid only when EOUT is low)	L	H	H	H	—	L
H	12	EOUT	I	Accepts operations from a CD or tuner	H	H	H	H	—	L
H	13	MUTE IN	I	Accepts a mute signal from an external input (effective only when EINI is low)	—	—	—	—	L	L
L	14	MUTE OUT	O	Mute output						L
H	15	RESET	I	Reset						L
5V	16	Vcc	—	Vcc (+5 V)						

CIRCUIT DESCRIPTION

IC506: MB88505PH Master microcomputer

The master microcomputer is used to control the operations of the entire system, including key input, display and loading/ejecting, and is also used for tuner control.



IC506: *Master microcomputer*

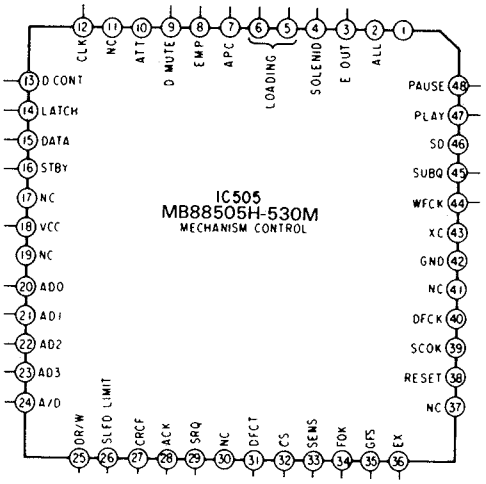
Pin No.	Pin Name	I/O	Functions
1	O_2	O	Display data and key scan output
2	O_3	O	Display data output
3	O_4	O	Display data output
4	CSI	O	Chip select output for mechanism control
5	DR/W	O	Data read/write select output
6	A/D	O	Address/data select output
7	—	—	Not used
8	A MUTE	O	Analog mute output
9	FLRESET	O	Reset output for FL display driver
10	—	—	—
11	—	—	—
12	R0	I/O	Address/data bus
13	R1	I/O	
14	R2	I/O	
15	R3	I/O	
16	START	I	Acc power voltage detection
17	—	—	—
18	+5 V		Vcc +5 V
19	—		—
20	ACK	I	Acknowledge input
21	SRQ	I	SRQ input
22	CLK	O	Clock output for FL display driver
23	CS2	O	Chip select signal output for extension port
24	RETURN	I	Return signal input

Pin No.	Pin Name	I/O	Functions
25	—	—	—
26	—	—	—
27	COL	O	Colon display ON/OFF signal output
28	D SW	I	"D" sensor signal input
29	E SW	I	"E" sensor signal input
30	NC	—	—
31	F SW	I	"F" switch signal input
32	K0	I	Key matrix signal input
33	K1	I	
34	K2	I	
35	K3	I	
36	EX	I	Clock oscillator pin
37	X	O	
38	RESET	I/O	Reset pin
39	REM IN	I	Remote input
40	TC	—	—
41	NC	—	—
42	GND	—	GND (Ground) pin
43	NC	—	—
44	PLL CLK	O	Data signal for the tuner PLL
45	PLL CHE	I	
46	PLL DATA	O	
47	O0	O	Display data and key scan output
48	O1	O	

CIRCUIT DESCRIPTION

IC505: MB88505H-530M Mechanism control microcomputer

The mechanism control microcomputer commands the servo control IC (IC502) and signal processing IC (IC503) to control the CD player. Also, pin 47 (PLAY), pin 48 (PAUSE), pin 3 (EOUT), pin 4 (plunger), and pins 5 and 6 (loading) function as extension ports of the master microcomputer.



IC505 Mechanism control microcomputer

Pin No.	Pin Name	I/O	Functions
1	—	—	—
2	—	—	—
3	EOUT	O	Remote output (when CD or TUNER is in operation)
4	Plunger	O	Plunger control output
5	Loading	O	Loading motor (forward/reverse) control output
6		O	
7	APC	O	Laser diode ON/OFF output
8	EMP	O	De-emphasis output
9	DMUTE	O	Digital muting output
10	—	—	—
11	NC	—	—
12	CLK	O	Clock output for IC502/IC503
13	DCONT	O	Control output for IC502
14	LATCH	O	Latch output for IC502/IC503
15	DATA	O	Data output for IC502/IC503
16	STBY	I	Standby input
17	NC	—	—
18	Vcc	—	Power supply (+5 V)
19	NC	—	—
20	AD0	I/O	Address and data bus
21	AD1	I/O	
22	AD2	I/O	
23	AD3	I/O	
24	A/D	I	Address/data select input

Pin No.	Pin Name	I/O	Functions
25	DR/W	I	Data read/write select input
26	Sled Limit	I	Sled (Feed) limit signal input
27	CRCF	I	CRC flag signal input
28	ACK	O	Acknowledge output
29	SRQ	O	SRQ output
30	NC	—	—
31	DFCT	I	Disc defect detection input
32	CS	I	Chip select input
33	SENS	I	Sense signal input
34	FOK	I	FOK signal input
35	GFS	I	GFS signal input
36	EX	I	Clock signal input
37	NC	—	—
38	RESET	I	Reset signal input
39	SCOR	I	SCOR signal input
40	DFCK	—	—
41	NC	—	—
42	GND	—	GND pin
43	XC	—	—
44	WFCK	I	WFCK signal input
45	SUBQ	I	SUBQ signal input
46	SD	—	Not used
47	PLAY	O	"PLAY" indication output
48	PAUSE	O	"PAUSE" indication output

MECHANISM OPERATION DESCRIPTION

Loading-in operation diagrams

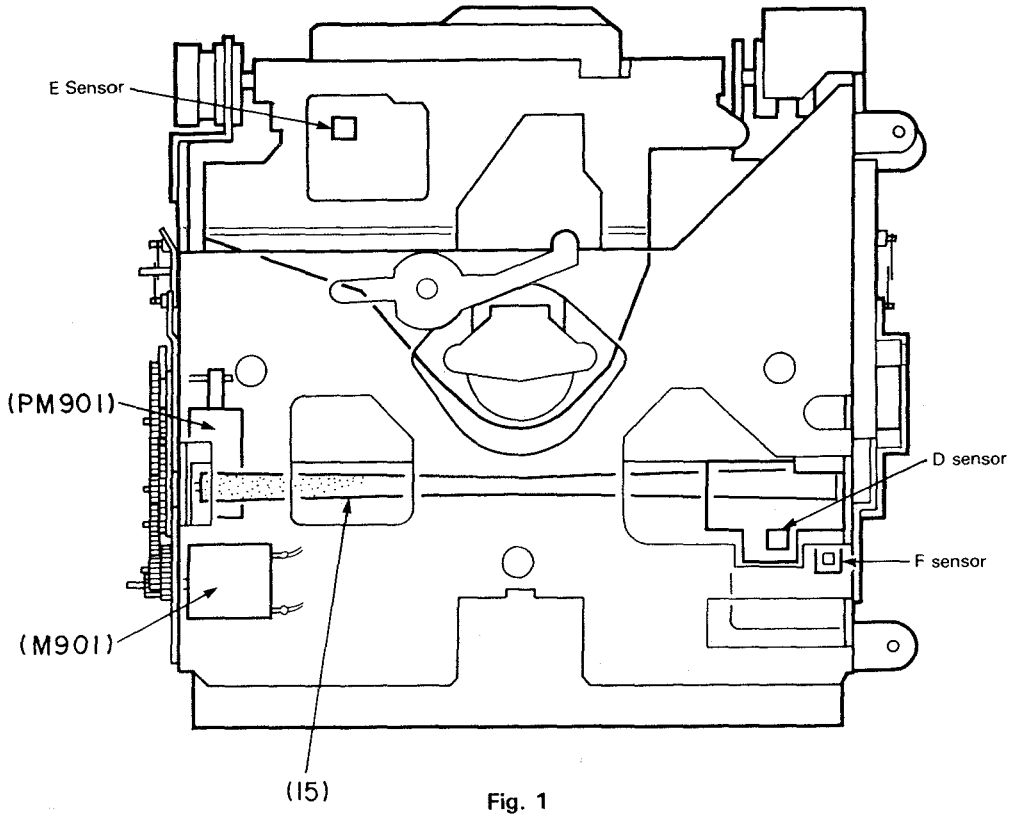


Fig. 1

1. When a disc is inserted in the direction of the arrow (❶), as shown in the figure on the right, the D sensor (❷) detects the inserted disc to start rotating the loading motor (❸).
   After this, gear (11), gear (10), the roller axis assembly gear (13) and gear (9) are rotated, in this order and in the direction of arrows (❹), (❺), (❻) and (❼) respectively.
   When the roller axis assembly is rotated, the inserted disc is loaded into the mechanism by the roller (15).
   At the same time, when gear (13) rotates, the reflection lever (8) is slightly inclined in the direction of the arrow (❽).

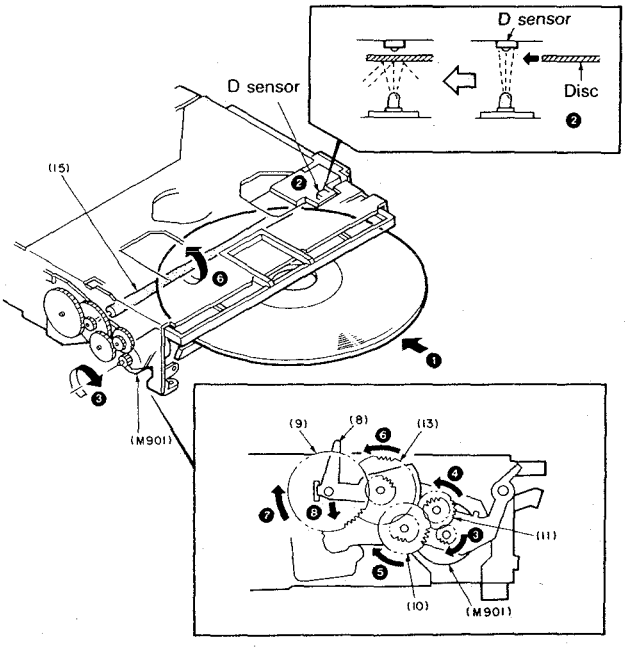


Fig. 2

MECHANISM OPERATION DESCRIPTION

2. When the disc comes to the E sensor (❾) position, the E sensor detects the disc end and pulls the plunger. Then the plunger shaft pulls the rack (14) in the direction of the arrow (❿), and the rack is connected to the inside of the gear (9) as indicated with the arrow (⓫).

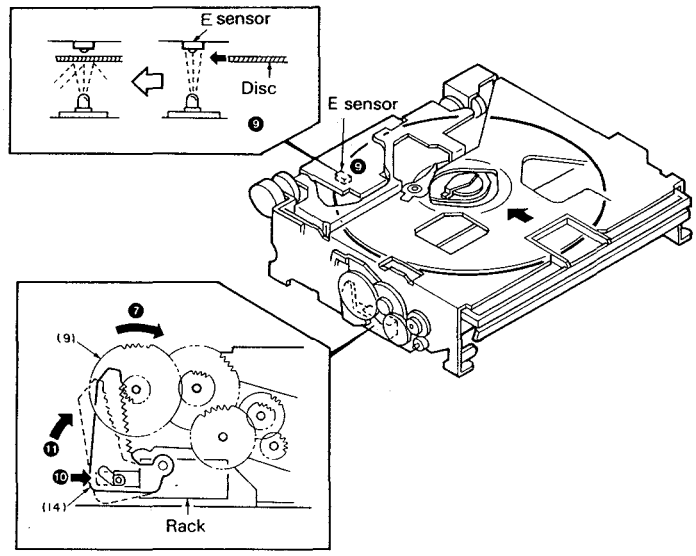


Fig. 3

3. By the operation shown in **Fig. 4**, gear (9), rotating in the direction of the arrow (❼), moves in the direction of the arrow (⓬) together with the drive/roller arm (23) and the support arm (6), along with the rack gear.
   At the same time, the disc shutter (52) attached to the drive/roller arm (23) moves in the direction of the arrow (⓭).
   * **Figures 5 to 7** show the operations which are activate simultaneously by the operation of the drive/roller arm.

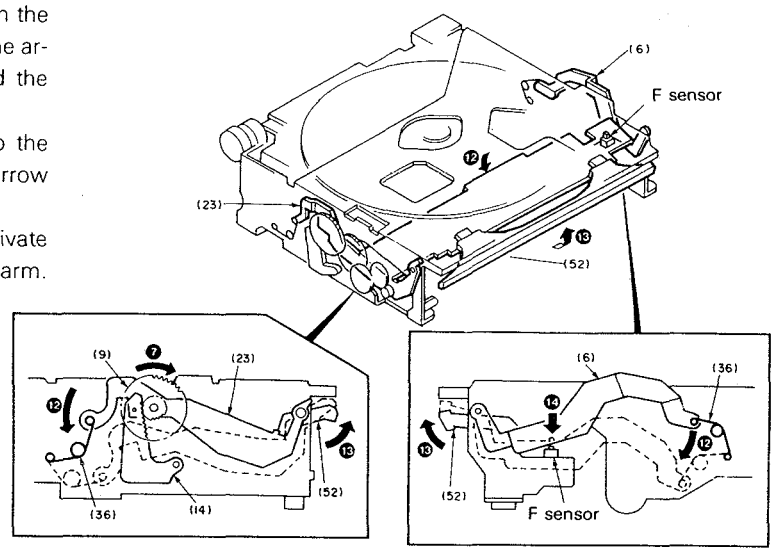


Fig. 4

4. While the drive/roller arm (23) is moving in the direction of the arrow (⓬), the shucking arm (7) also moves as shown in the figure, so that the disc is securely held on the turntable.

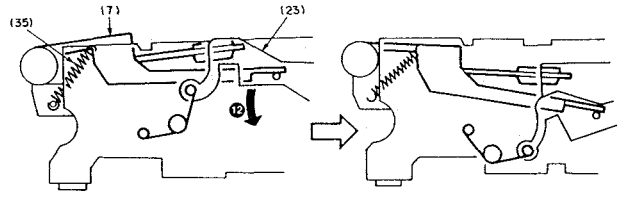


Fig. 5

MECHANISM OPERATION DESCRIPTION

5. When the drive/roller arm (23) moves in the direction of the arrow (⓬), the metal fitting rotates in the direction of arrow (Ⓐ), to release the MD (mechanism deck) mount securing shaft, as shown in the figure.

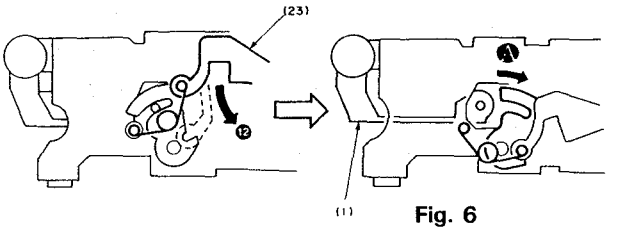


Fig. 6

6. When the support arm moves in the direction of the arrow (⓬), it moves the metal fitting in the direction of arrow (Ⓐ). And, at the same time, when the lock hook (21) moves in the direction of arrow (Ⓑ), the securing shaft which protrudes from the MD (mechanism deck) mount chassis is released at the two positions.

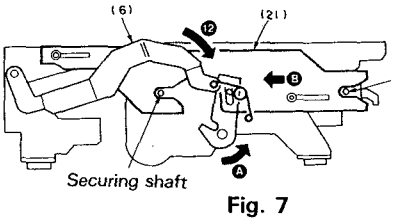


Fig. 7

Loading-out operation diagrams

1. When the eject switch is pushed, the loading motor (M901) starts rotating in the direction of the arrow. (❶)
   When the loading motor rotates, gears (11), (10), (13) and (9) start rotating in the direction of arrows (❷), (❸), (❹) and (❺) respectively.
   As the gear inside of gear (9) is lifted up along with the rack (14), the drive/roller arm (23) moves in the direction of the arrow (❻).

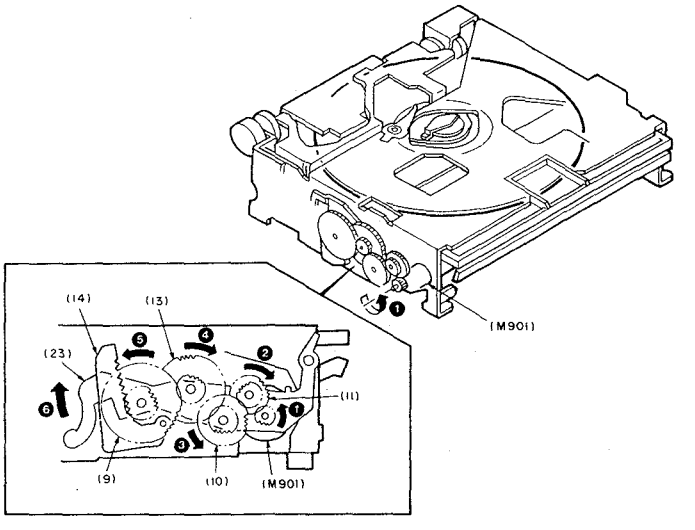


Fig. 8

2. At the same time, the support arm (6) secured to the drive/roller arm (23) also moves in the direction of the arrow (6).
   When gear (9) is released from the rack, the drive/roller arm (23) and the support arm (❻) are secured by the roller/drive spring (36).
   At the same time, the disc shutter (52), which is secured to the drive/roller arm (23), moves in the direction of the arrow (❼) and opens.
   * **Figures 10 to 12** show the operations which are activate simultaneously by the operation of the drive/roller arm (and support arm).

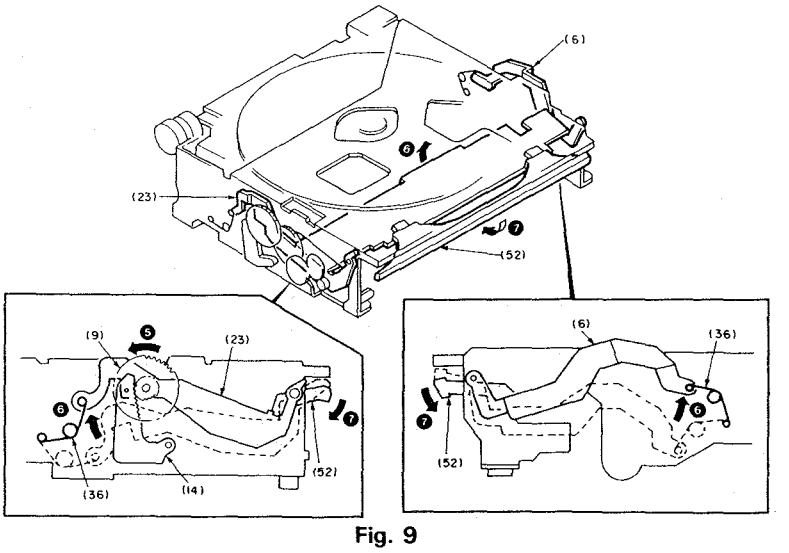


Fig. 9

MECHANISM OPERATION DESCRIPTION

3. While the drive/roller arm (23) is operating (❻), the metal fitting rotates in the direction of arrow (Ⓐ), to secure the shaft of the MD mount chassis (1), as shown in the figure. (Ⓑ)

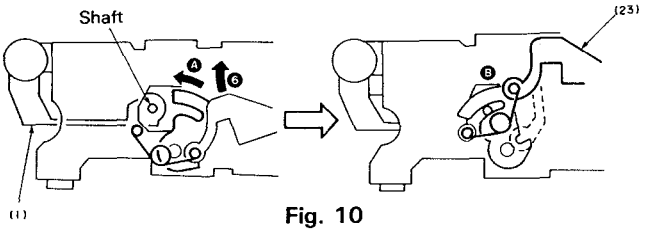


Fig. 10

4. While the support arm (❻) is operating, the metal fitting rotates in the direction of arrow (Ⓐ), to shift the lock hook (21) in the direction of arrow (Ⓑ) so that the shaft of the MD mount chassis (1) is secured.

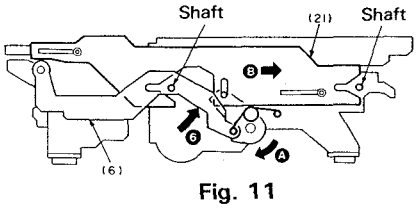


Fig. 11

5. While the drive/roller arm (23) is operating (❻), the chucking arm (7) also moves in the direction of the arrow (❼), to release the disc held on the turntable, as shown in the figure.

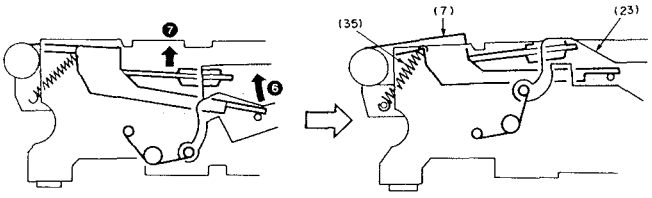


Fig. 12

6. After the drive/roller arm (23) has operated, the roller (15) beneath the disc is rotated in the direction of the arrow (❽) to eject the disc. (❾)
Then, when the D sensor detects the disc passing through the D sensor (❿) position, the loading motor (M201) is turned OFF and the loading-out operation is completed.

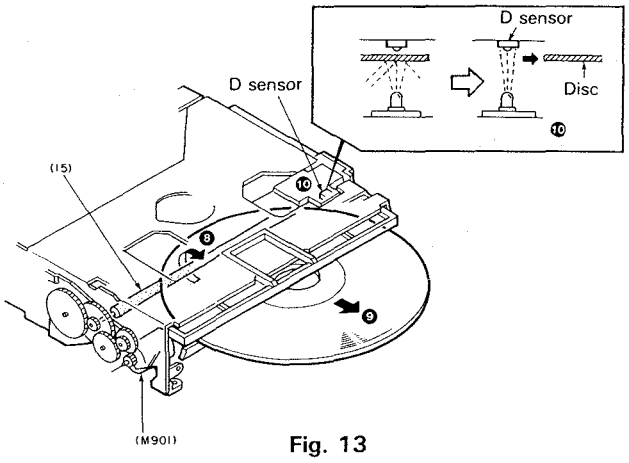


Fig. 13

ADJUSTMENT

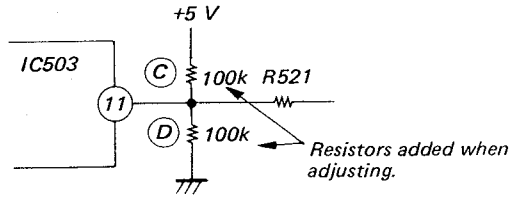
1. Perform adjustments as given.
2. Be sure to use the disc "YEDS-18"

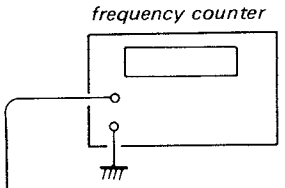
3. Power supply voltage: DC 14.4 V (more than 2A)

PLL Free Run Frequency Adjustment

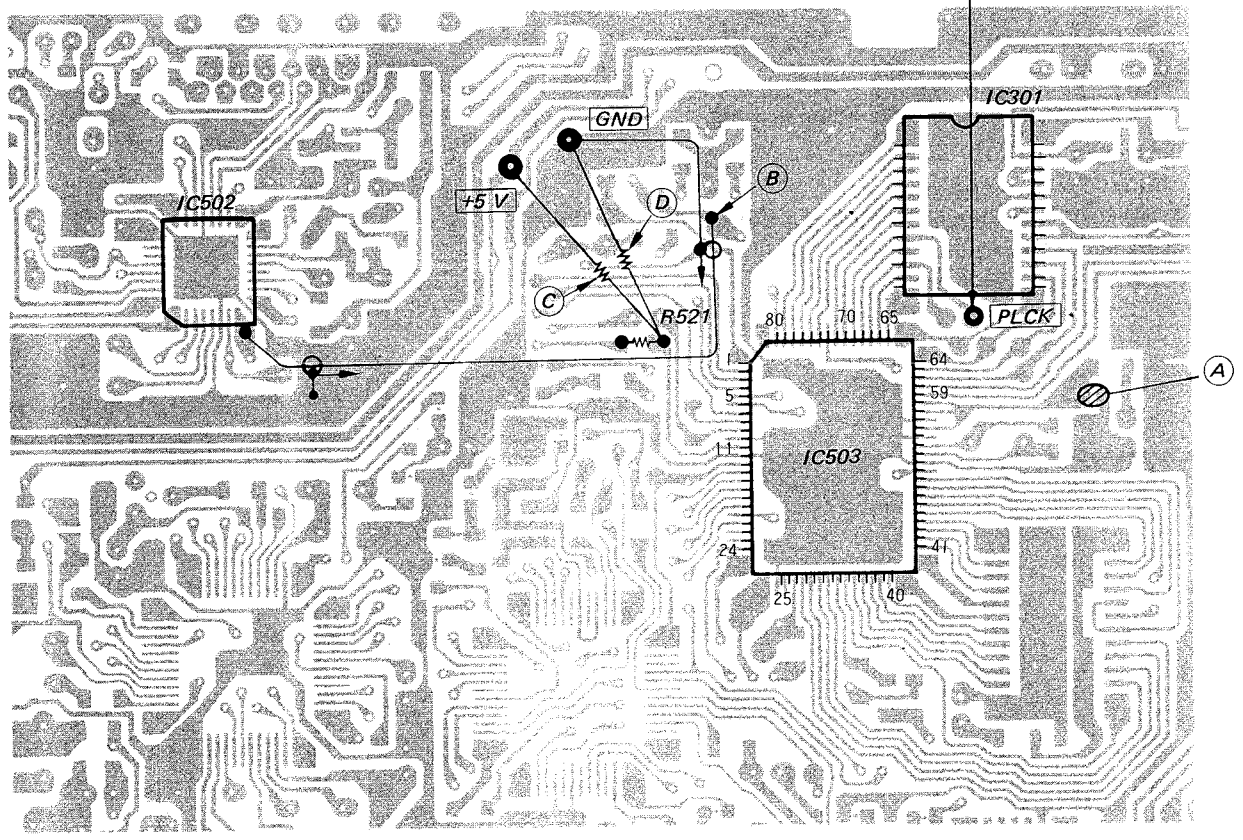
Procedure:

1. Solder-bridge the main board point Ⓐ. (IC503 pin 59 is grounded)
2. Remove main board point Ⓑ leads. (Disconnect IC503 pin 5)
3. Connect 100 kΩ resistors to Ⓒ, Ⓓ. (This is to adjust the IC503 pin 11 voltage to 2.5 V)
4. Connect the frequency counter to main board test point PLCK (IC503 pin 70).
5. Turn the power switch on (Do not use the disc), then adjust RV505 so that the frequency is 4.3218 MHz ±10 kHz.
6. After adjusting, reset 1, 2 and 3 as original.





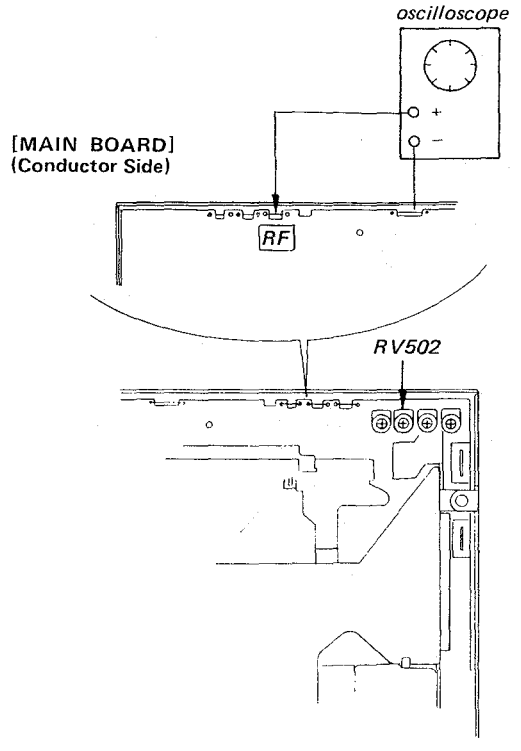
[MAIN BOARD]



ADJUSTMENT

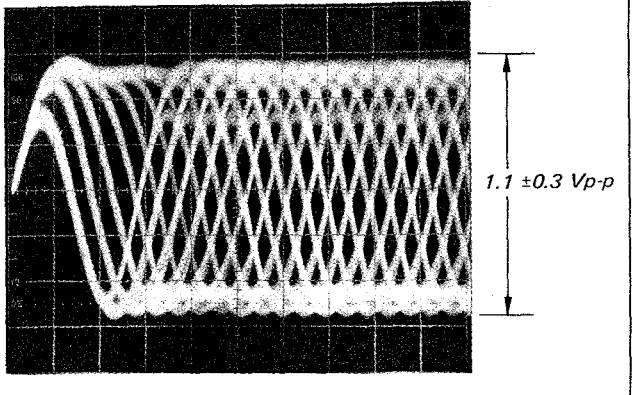
Focus Offset Adjustment

Procedure:



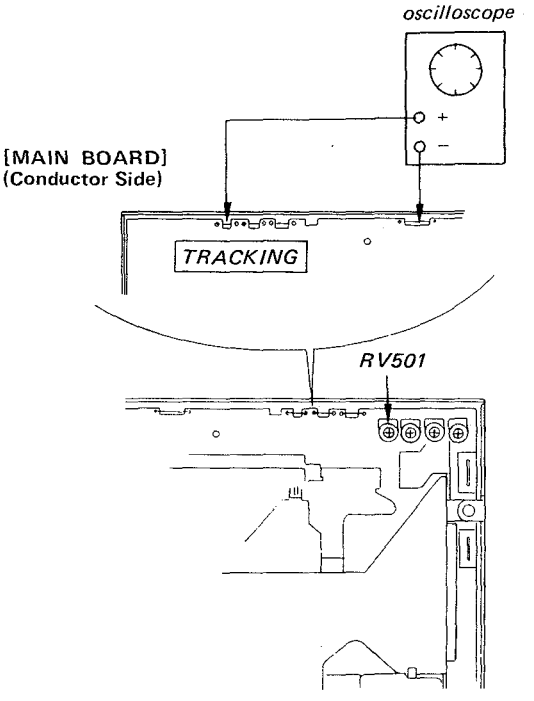
1. Connect the oscilloscope to main board test point RF.
2. Put the set into play mode by loading the disc.
3. Adjust main board RV502 so that the oscilloscope waveform eye pattern is good.
   A good eye pattern means that the diamond shape (◇) in the center of the oscilloscope can be clearly distinguished.

Volt/Div: 200 mV
Time/Div: 0.5 µSec



Tracking Offset Adjustment

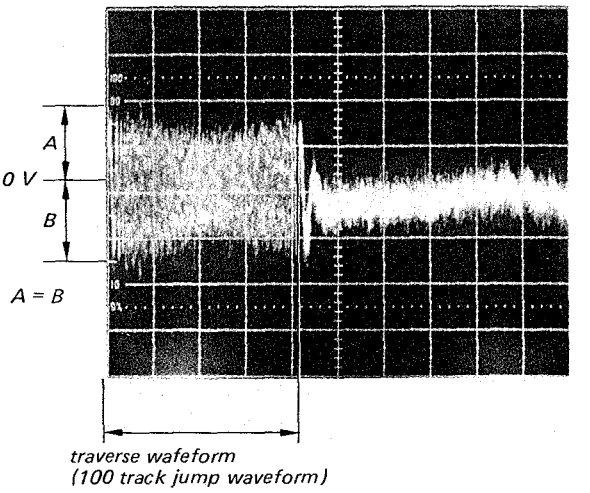
Procedure:



1. Connect the oscilloscope to main board test point TRACKING.
2. Put the set into play mode by loading the disc.
3. Press the ⏮ or ⏭ (or ◀◀ , ▶▶) button, then check the traverse waveform*.
4. Adjust RV501 (main board) so that oscilloscope reading is symmetrical in relation to 0 V.

*Traverse waveform: This is the tracking error waveform appears when crossing the track.

Volt/Div: 0.5 V
Time Div: 2 mSec
Center 0 V



traverse wafeform
(100 track jump waveform)

ADJUSTMENT

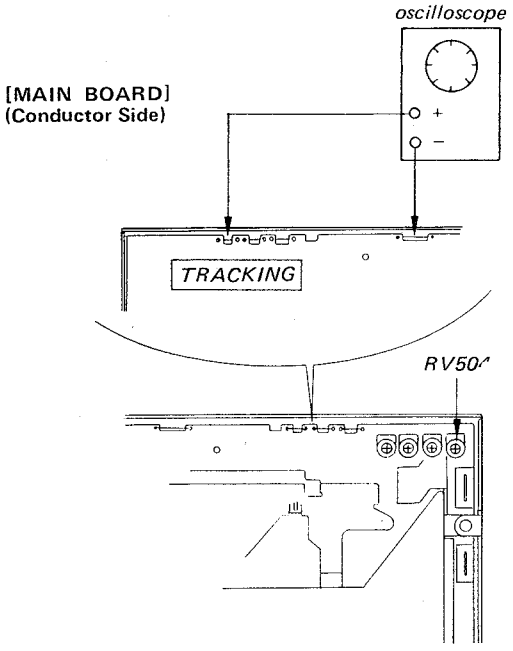
Tracking Gain Adjustment (rough adjustment)

This adjustment is to be performed when replacing the following parts.

- Optical Pick-up Block
- RV504

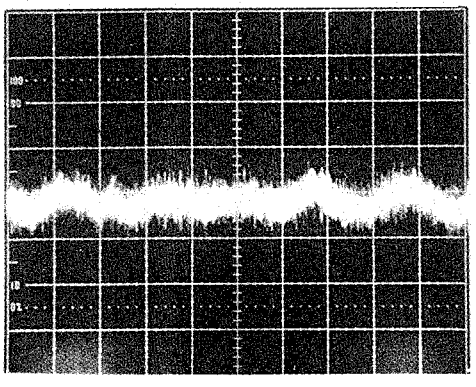
This adjustment should be performed after focus offset and tracking offset adjustment is completed.

Procedure:

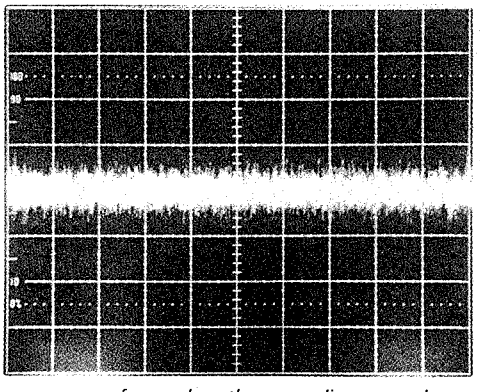


1. Connect the oscilloscope to main board test point TRACKING .
2. Put the set into play mode by loading the disc.
3. Turn main board RV504 counterclockwise, then check the ocilloscope waveform.
   Fix RV504 to the position that the waveform disappears.

Volt/Div: 0.5 V
Time/Div: 2 mSec

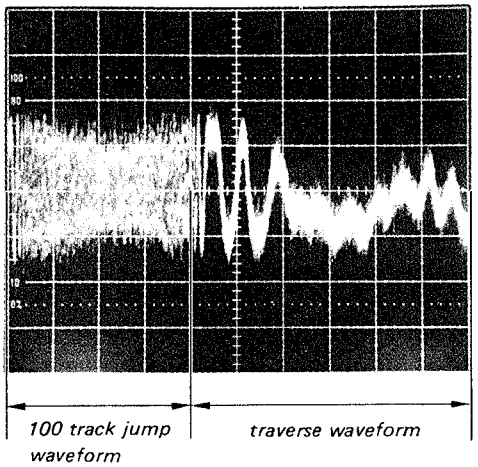


waveform when the wave appears

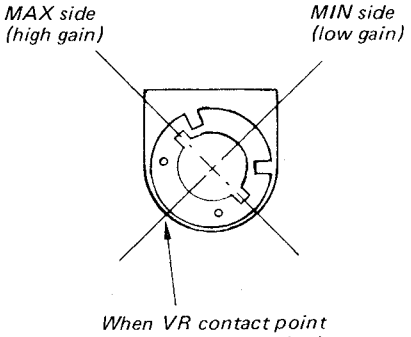


waveform when the wave disappeared

- **When gain is lowered . . .**
  When selecting by pressing |◀◀ or ▶▶| button, brake application is poor because of low tracking gain. Therefore, the traverse waveform appears after the 100 track jump waveform, then the selection will be located slowly.



- **When gain is highered . . .**
  Operation noise is heard due to a scratch or dust, then operation will be instability.



RV503 standard position

ADJUSTMENT/VOLTAGE TABLES

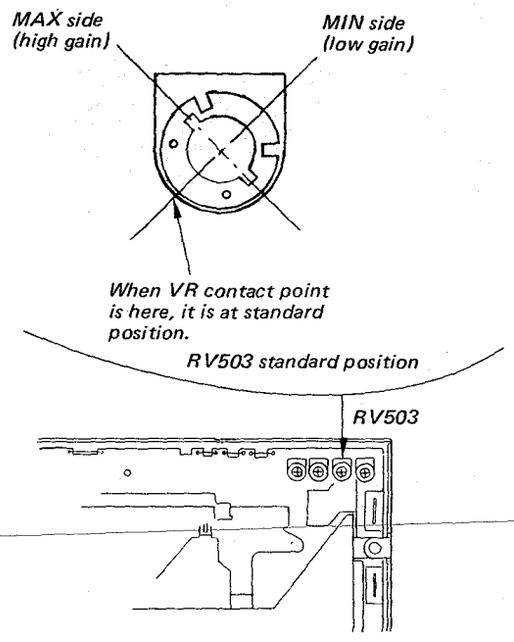
Focus Gain Adjustment (rough adjustment)

This adjustment is to be performed when replacing the following parts.

- Optical Pick-up Block
- RV503

Procedure:

1. Set RV503 (main board) to the standard position.
2. Check that there is not an abnormal amount of operation noise (white noise) from the 2-axis devise. If there is, turn RV503 slightly counter-clockwise.



- **When gain is lowered . . .**
  The set does not play because of no focus operation.
- **When gian is highered . . .**
  Operation noise is heard due to a scratch or a dust, then operation will be instability.

MOTHER UNIT IC

IC201, 101

1~3	0V
4	-4.9V
5,6	0V
8	4.9V

IC202, 102

1	4.7V
2,3	0V
4	-4.9V
5~7	0V
8	4.9V

IC301

1~16	2.5V
17~19	0V
20	–
21,22	0V
23,24	4.9V

IC302

1,3,4,15	0V
7	-4.9V
9,10	1.2V
16	4.9V

IC303

1,3	0V
7	-4.9V
9,10	5.1V
16	4.9V

IC501

1	0V	17	5V
2	-4.2V	18	-5V
3	0V	19	0V
4	1.2V	20	0V
5	0.3V	21	0V
6	–	22	0V
7	2.5V	23	0V
8	2.5V	24	-0.5V
9	5V	25	-0.3V
10	0.4V	26	–
11	5.2V	27	–
12	–	28	-1.3V
13	0V	29	-1.1V
14	0.7V	30	-5.2V
15	0V	31	0.1V
16	–	32	0V

IC502

1	–	26	–
2~4	0V	27,28	2.6V
5	-1.2V	29	-2.3V
6	0V	30	2.4V
7	0.9V	31	3.6V
8,9	0V	32	2.3V
10	5.2V	33	5.2V
11	0.1V	34	2.5V
12,13	0V	35	5.1V
14	0.3V	36	2.6V
15	0V	37	5.2V
16	–	38	0V
17	-4.1V	39	0.7V
18	5V	40	2.6V
19	-5.2V	41	–
20	0.1V	42	0V
21	5.2V	43	-5.2V
22,23	5V	44	-4.2V
24,25	5.1V	45~48	0V

IC503

1	0V	24	0V	60,61	1.2V
2	5.1V	25	2.6V	62~72	2.5V
3	2.5V	26,27	–	73	5.2V
4	2.8V	28	5.1V	74~78	2.5V
5,6	2.5V	29~32	1.9V	79	2.6V
7	5.2V	33	5.2V	80	–
8	2.5V	34~37	1.9V		
9	2.4V	38~45	2.5V		
10,12	–	46,47	2.6V		
11	1.7V	48	2.5V		
13,14	5.1V	49	4.6V		
15,16	5V	50	2.7V		
17	0.1V	51	2.1V		
18	5V	52	–		
19	0V	53	0.7V		
20	5.2V	54	2V		
21,22	–	55,57	–		
23	1.5V	56,58,59	5.1V		

IC504

1	–
2	5V
3	–
4	-5V
5~8	–

IC505

1,2	–	28,29,31	5.1V
3	0V	30	–
4	5.1V	32	4.9V
5,6	5.2V	33,34	5V
7	0V	35	5.1V
8	5.1V	36	2.5V
9	0V	37	2.1V
10,11	–	38	5V
12~16,18	5.1V	39	0V
17	–	40~43	–
19	2.8V	44	2.6V
20	5.1V	45	1.4V
21	0V	46	1.3V
22~26	5.1V	47	0V
27	5.2V	48	5.1V

IC506

1	4.3V	23,24	5V	46	5V
2	0.2V	25,26	–	47,48	0.5V
3,4	5V	27	0V		
5,6	5.1V	28,29	5V		
7	–	30	–		
8	0V	31	0V		
9	5V	32~35	4V		
10,11	–	36	1.1V		
12~16	5.1V	37	2.2V		
17	–	38	5V		
18	5.1V	39	4.8V		
19	–	40~43	–		
20,21	5.1V	44	5V		
22	0V	45	0V		

IC507

1~8	2.5V
9~11	1.9V
13~17	
12	–
18	2.7V
19	2.5V
20	2.7V
21	4.6V
22,23	2.6V
24	5.2V

IC508

1	30V
2	5.2V
3	1.4V
4	0.5V
5	4.3V
6	0.2V
7	5V
8	–
9	0V
10	5V
11	5.2V
12	5V
13	–
14	–
15	2.1V
16	–
17~24	*1
25~32	3.2V

IC509

1	4.1V
2~5	5.1V
6	5V
7~11	5.1V
12	–
13~16	5.1V
17,18	–
19,20	5.1V
21	–
22~24	5.1V

IC510

1	5.1V
2	1.7V
3	5.1V
4	3.7V
5	5.1V
6~10	–
11	5.1V
12	3.7V
13	5.1V
14	–
15	5V
16	5.2V

IC512

1,2	5.1V	9	0V
3	4.7V	10	0V
4	4.8V	11	5.1V
5	5.1V	12	0V
6	3.8V	13	5.1V
7	2.5V	14	3.7V
8	–	15	5V
		16	5.2V

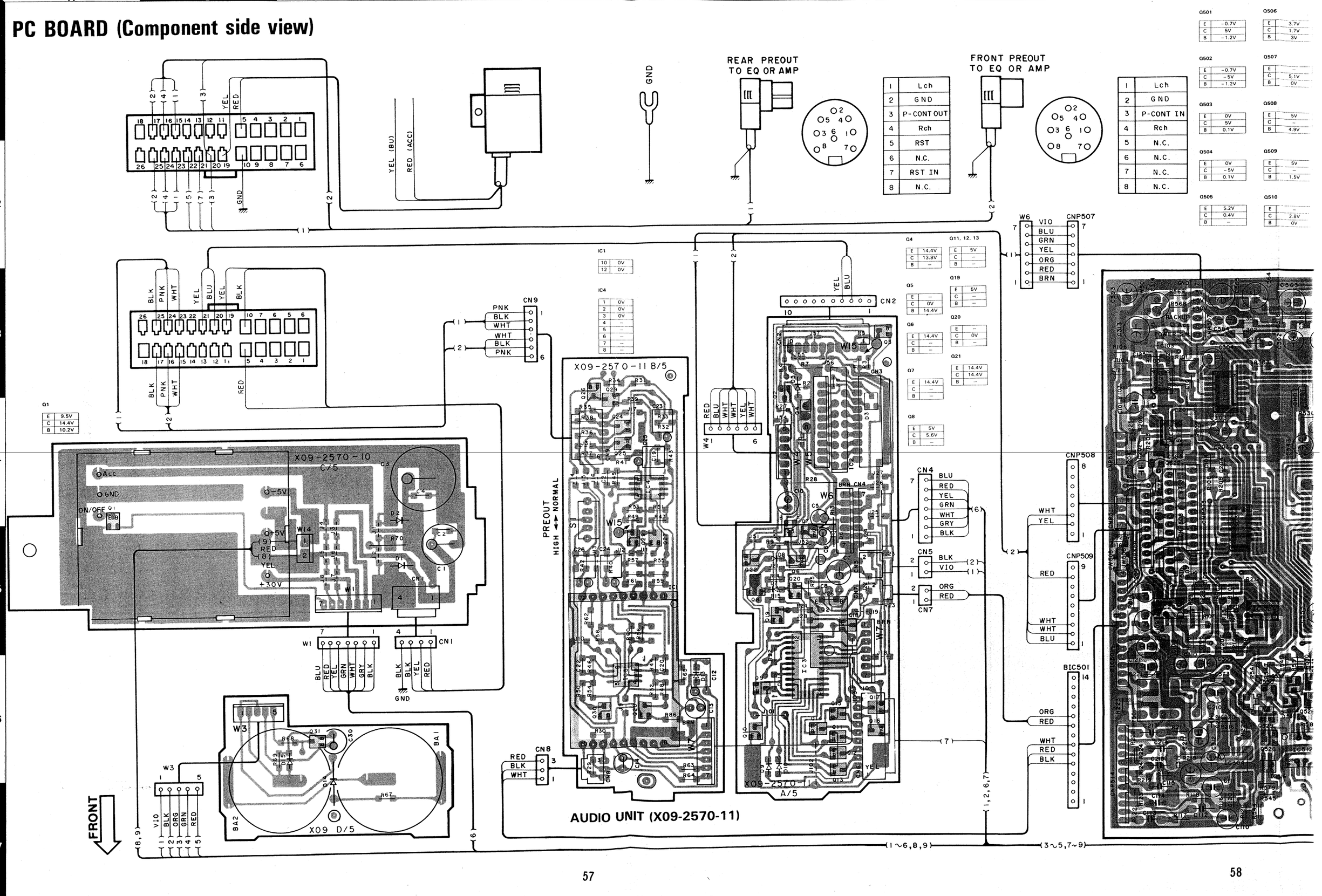
IC513

1	5V
2,3	0V
4	4.6V
7	–
10	4.7V
11,12	0V
13	5V
14	5.2V

IC514

1	5V
2	5.2V
3	–

PC BOARD (Component side view)



Q1

E	9.5V
C	14.4V
B	10.2V

IC1

10	0V
12	0V

IC4

1	0V
2	0V
3	0V
4	—
5	—
6	—
7	—
8	—

1	Lch
2	GND
3	P-CONT OUT
4	Rch
5	RST
6	N.C.
7	RST IN
8	N.C.

1	Lch
2	GND
3	P-CONT IN
4	Rch
5	N.C.
6	N.C.
7	N.C.
8	N.C.

Q4

E	14.4V
C	13.8V
B	—

Q11, 12, 13

E	5V
C	—
B	—

Q5

E	—
C	0V
B	14.4V

Q19

E	5V
C	—
B	—

Q6

E	14.4V
C	—
B	—

Q20

E	—
C	0V
B	—

Q7

E	14.4V
C	—
B	—

Q21

E	14.4V
C	14.4V
B	—

Q8

E	5V
C	5.6V
B	—

Q501

E	-0.7V
C	5V
B	-1.2V

Q506

E	3.7V
C	1.7V
B	3V

Q502

E	-0.7V
C	-5V
B	-1.2V

Q507

E	—
C	5.1V
B	0V

Q503

E	0V
C	5V
B	0.1V

Q508

E	5V
C	—
B	4.9V

Q504

E	0V
C	-5V
B	0.1V

Q509

E	5V
C	—
B	1.5V

Q505

E	5.2V
C	0.4V
B	—

Q510

E	—
C	2.8V
B	0V

Q501

E	−0.7V
C	5V
B	−1.2V

Q502

E	−0.7V
C	−5V
B	−1.2V

Q503

E	0V
C	5V
B	0.1V

Q504

E	0V
C	−5V
B	0.1V

Q505

E	5.2V
C	0.4V
B	—

Q506

E	3.7V
C	1.7V
B	3V

Q507

E	—
C	5.1V
B	0V

Q508

E	5V
C	—
B	4.9V

Q509

E	5V
C	—
B	1.5V

Q510

E	—
C	2.8V
B	0V

Q511

E	—
C	6V
B	2.8V

Q512, 513

E	5.2V
C	0V
B	5.1V

Q514

E	0.8V ((3.6))V
C	—
B	0V ((5.2))V

Q515

E	3.7V
C	—
B	5.2V

Q517

E	5.2V
C	—
B	—

Q518

E	—
C	0V
B	0.6V

Q519

E	—
C	14.2V
B	0V

Q520

E	5.1V
C	13.5V
B	5.6V

Q522

E	—
C	0V
B	4.8V

Q523

E	14.4V
C	14.4V
B	0V

Q524

E	—
C	0V
B	3.8V

Q525

E	14.4V
C	—
B	5V

Q526

E	—
C	5V
B	0.6V

Q528

E	—
C	0V
B	3.7V

Q529

E	0V
C	0.2V
B	5.7V

Q530

E	—
C	5.1V
B	0V

Q531

E	—
C	5.1V
B	0V

Q532

E	—
C	5.1V
B	0V

Q533

E	19.5V
C	0V
B	19V

Q534

E	—
C	19V
B	0V

Q536

E	5.2V
C	0V LOAD:5V
B	5.2V LOAD:0V

Q537

E	5.2V
C	0V UNLOAD:5V
B	5.2V UNLOAD:0V

Q538

E	—
C	0V UNLOAD:5V
B	0V LOAD:5V

Q539

E	—
C	0V LOAD:5V
B	0V UNLOAD:5V

Q540

E	0V
C	5.2V
B	4.2V

Q541

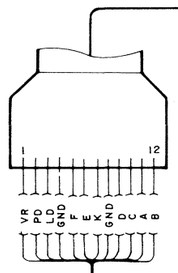
E	2.8V
C	—
B	5.1V

Q902

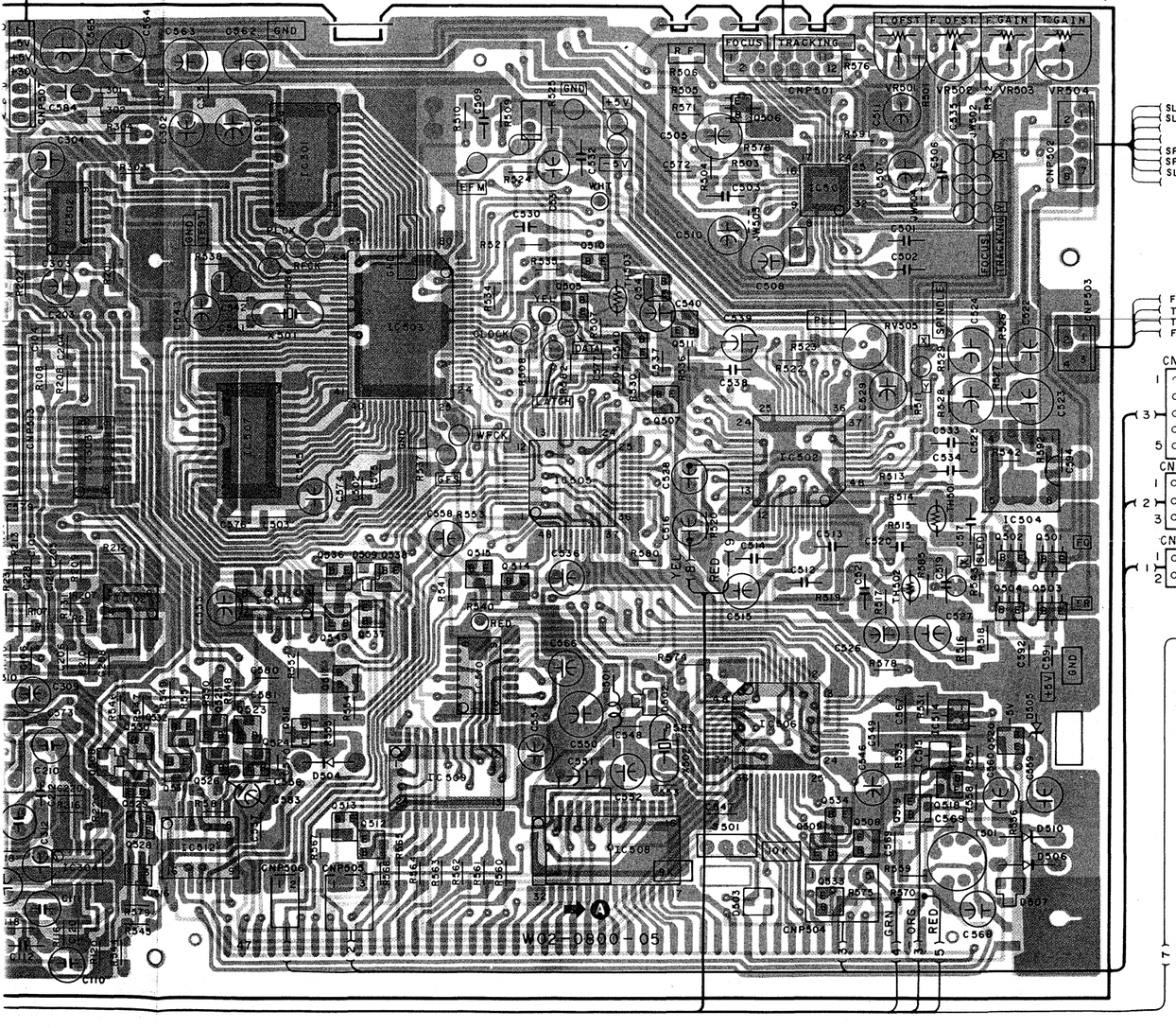
E	—
C	4.9V

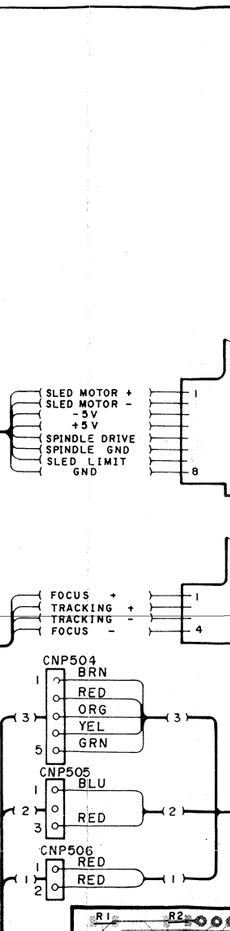
Q901

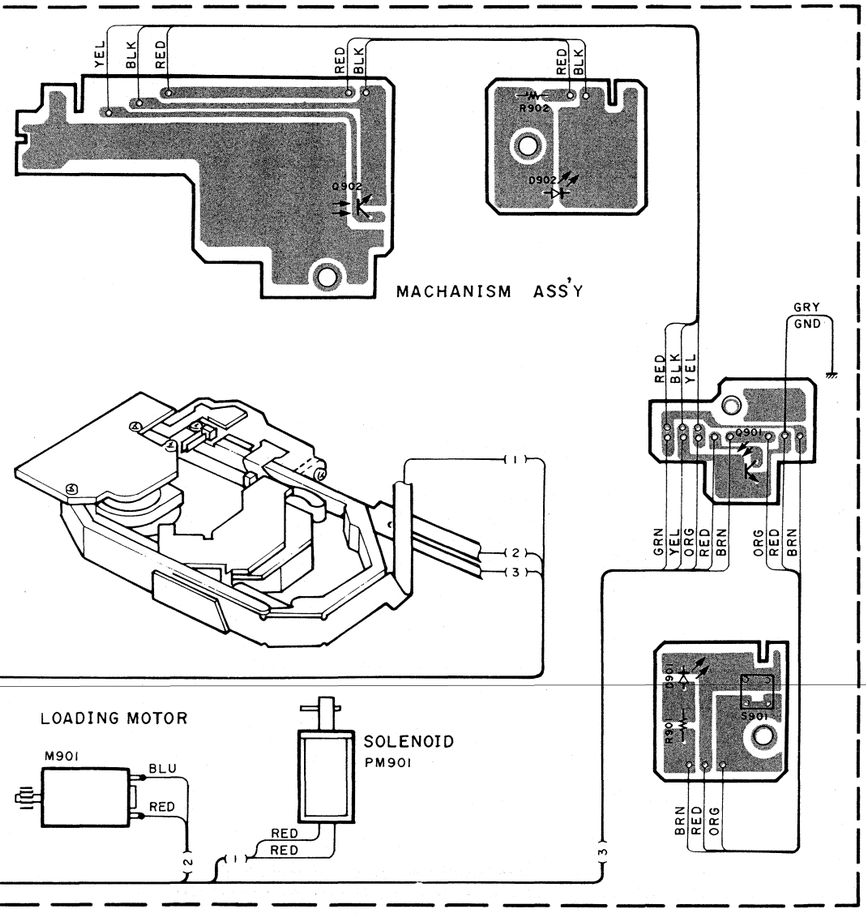
E	—
C	1.5V



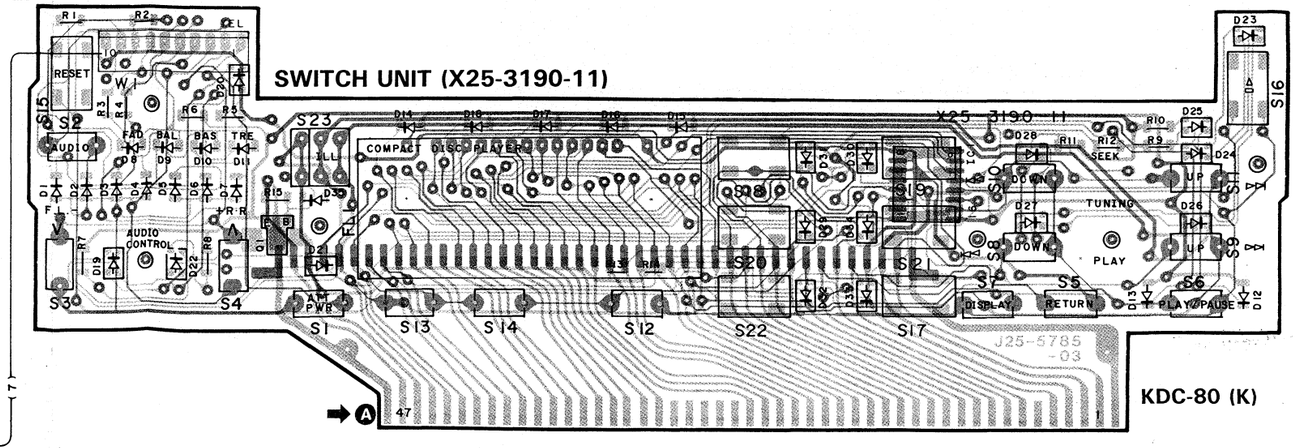
MOTHER UNIT (W02-0800-05)







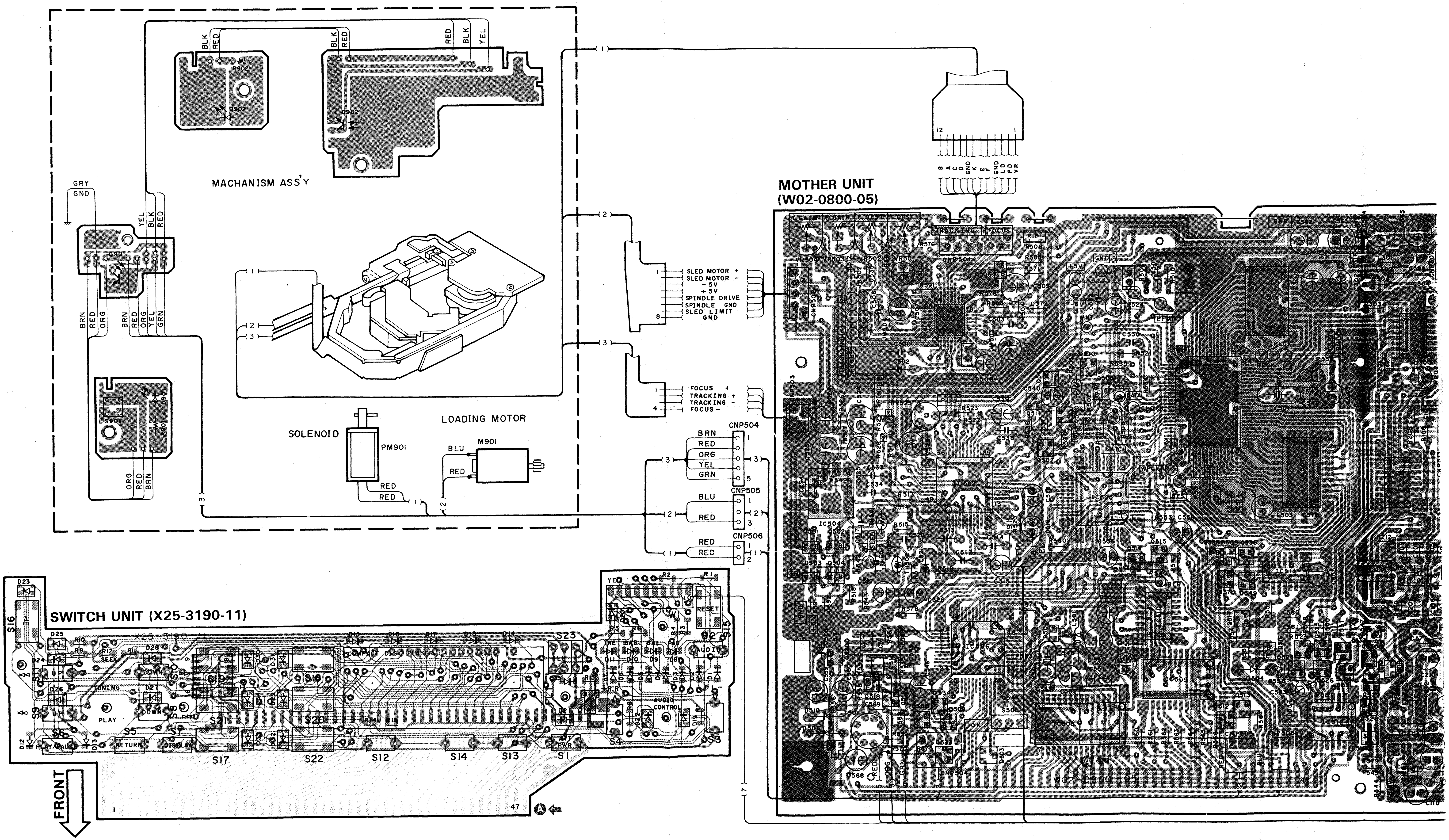
SWITCH UNIT (X25-3190-11)



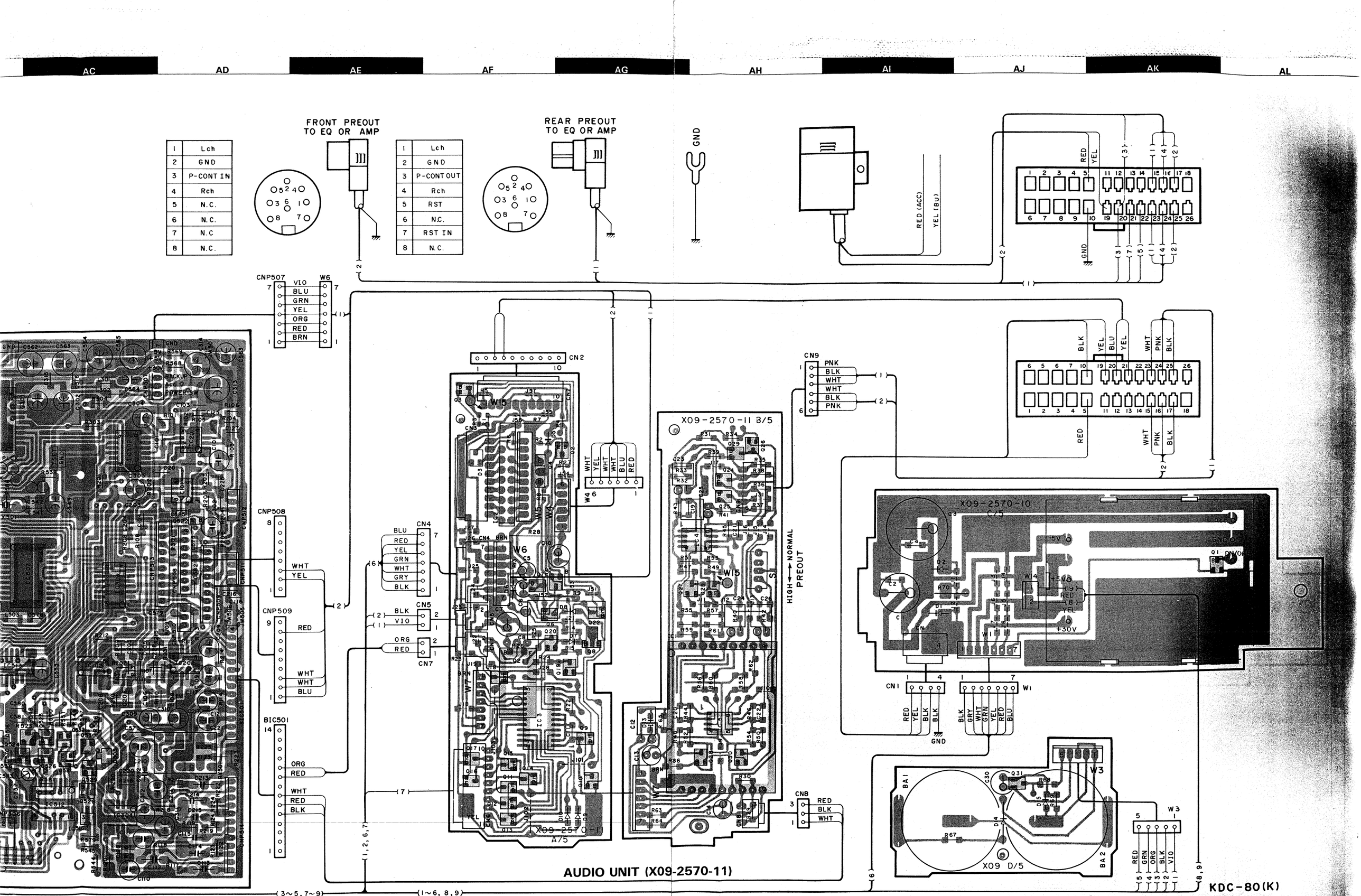
KDC-80 (K)

Refer to the schematic diagram for the values of resistors and capacitors.

PC BOARD (Foil side view)



MACHANISM ASS'Y
R902
D902
Q902
Q901
S901
D901
R901
GRY
GND
BLK
RED
YEL
BRN
ORG
GRN
SOLENOID
PM901
LOADING MOTOR
M901
BLU
SLED MOTOR +
SLED MOTOR -
- 5V
+ 5V
SPINDLE DRIVE
SPINDLE GND
SLED LIMIT
GND
FOCUS +
TRACKING +
TRACKING -
FOCUS -
CNP504
CNP505
CNP506
MOTHER UNIT
(W02-0800-05)
B A C D GND K E F GND LD PD VR
T.GAIN
F.GAIN
F.OFST
T.OFST
TRACKING
FOCUS
CNP501
IC501
IC502
IC503
IC504
IC505
IC506
IC508
IC509
IC512
IC513
X501
SWITCH UNIT (X25-3190-11)
SEEK
UP
DOWN
TUNING
PLAY
PLAY/PAUSE
RETURN
DISPLAY
COMPACT DISC PLAYER
RESET
AUDIO
AUDIO CONTROL
ATT PWR
S1
S3
S4
S5
S6
S7
S9
S12
S13
S14
S16
S17
S18
S20
S21
S22
S23
FRONT



AUDIO UNIT (X09-2570-11)

KDC-80(K)

Refer to the schematic diagram for the values of resistors and capacitors.

【MAIN BOARD】

KSS-160B
OPTICAL
PICK-UP(1/2)

LASER DIODE

DITECTOR

Q506
2SB1123
APC DRIVE

IC501 CXA1081Q
RF AMP, SIGNAL PROCESSER
LASER ON CIRCUIT, MIDPOINT VOLTAGE GENERATOR

Q505
2SA1179
COMPARATOR

Q510 2SC3395
PLL BAND SELECT

Q511 2SC3398
PLL BAND SELECT

Q541 2SA1510
PLL BAND SELECT

IC503 CXD1130Q
SIGNAL PROCESSOR

IC507 CXK5816
RAM

IC301 PCM55HP-S
D/A CONVERTER

IC302 TC40538F
ANALOG SWITCH

IC502
CXA1082Q
FOCUS/TRACKING/SLED/CLV SERVO

IC505
MB88505-530M
MECHANISM CONTROL

IC504
L272M
MOTOR DRIVE

Q501,503 Q502,504
2SD1623 2SB1123
SERVO DRIVER

Q536,537 Q538,539
DTB113EK DTD113ZK
LOADING MOTOR DRIVE

Q51 2SA1179
SOLENOID SWITCH

Q516 2SD1623
SOLENOID DRIVE

Q514,515
2SA1179
LED SWITCH

Q540 2SC2812
DEFECT BUFFER

Q507 2SC2812
DEFECT DETECT

IC514
S-8054HNCB
RESET

Q902
PN147-LF-R
DISC SENSOR

D504
V06C

D902
TLR123

D901 TLR123

S901
SHUTTER DET
(ON:WHEN SHUTTER IS CLOSED)

SPINDLE MOTOR
(MD SLED CASSIS)

KSS-160B
OPTICAL
PICK-UP(1/2)

DTA144WK
DTB113EK
DTB123YK
DTD113ZK
2SA1179
2SA1344
2SA1510
2SB1123
2SC2812
2SC3395
2SC3398

2SD1623

MB88201-534M

S-8054HN

CXK5816

L272M

LC74HC365M

TC4053BF

LC74HC04M

PCM55HP-S

CXD1130Q

CXA1082AQ
MB88505-502M

M5203FP

M54940FP

CXA1081Q
μPD82C43G

DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

Les tensions c.c. doivent être mesurées avec un voltmètre à haute impédance. Les valeurs peuvent différer légèrement du fait des variations inhérentes aux appareils et aux instruments de mesure individuels.

a high impedance due to variations units.

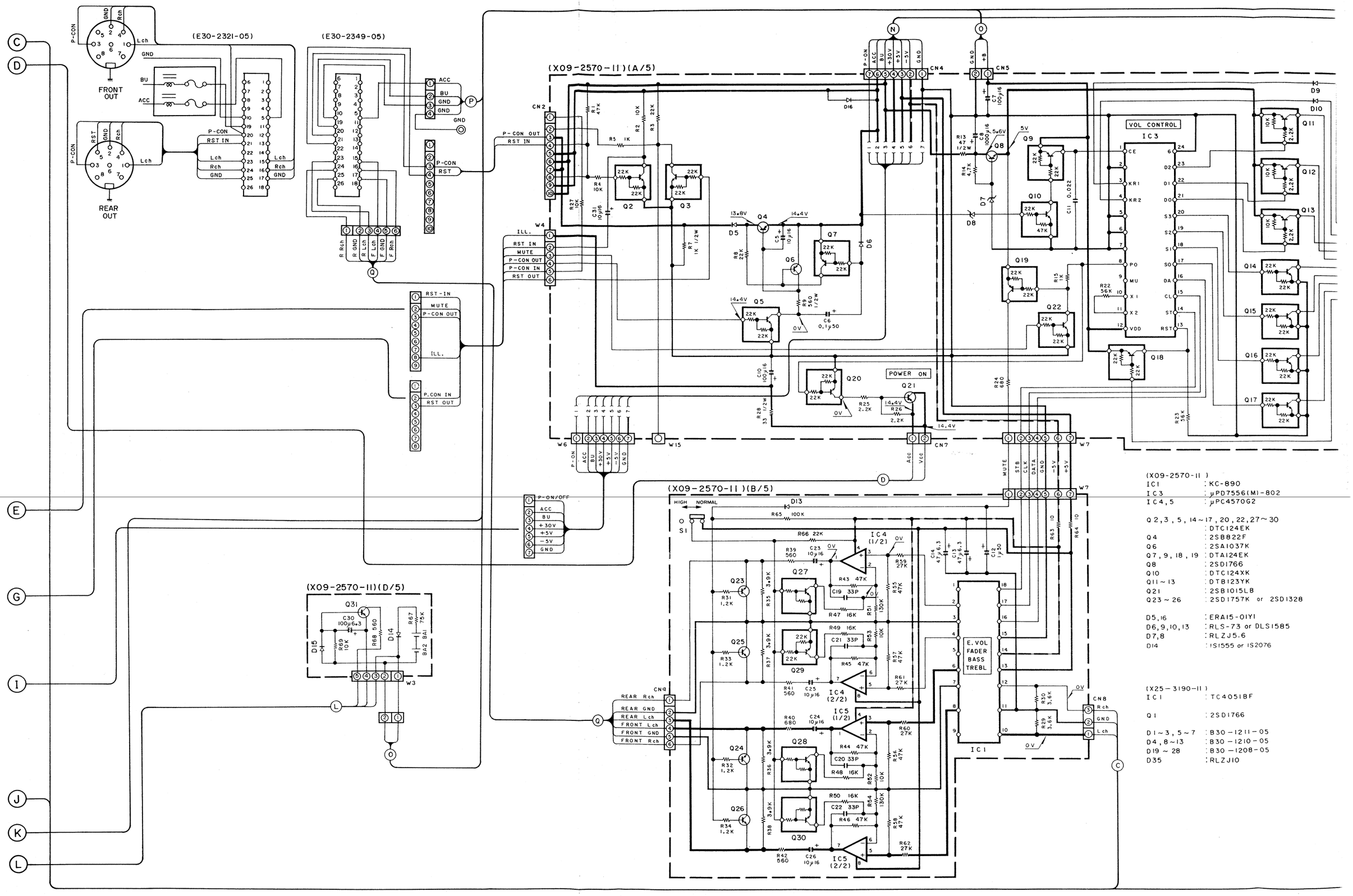
ées avec un volt- rs peuvent différer s inhérentes aux individuels.

Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen Spannungsmesser gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen Instrumenten oder Geräten u.U. geringfügig.

CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

KDC-80

KENWOOD

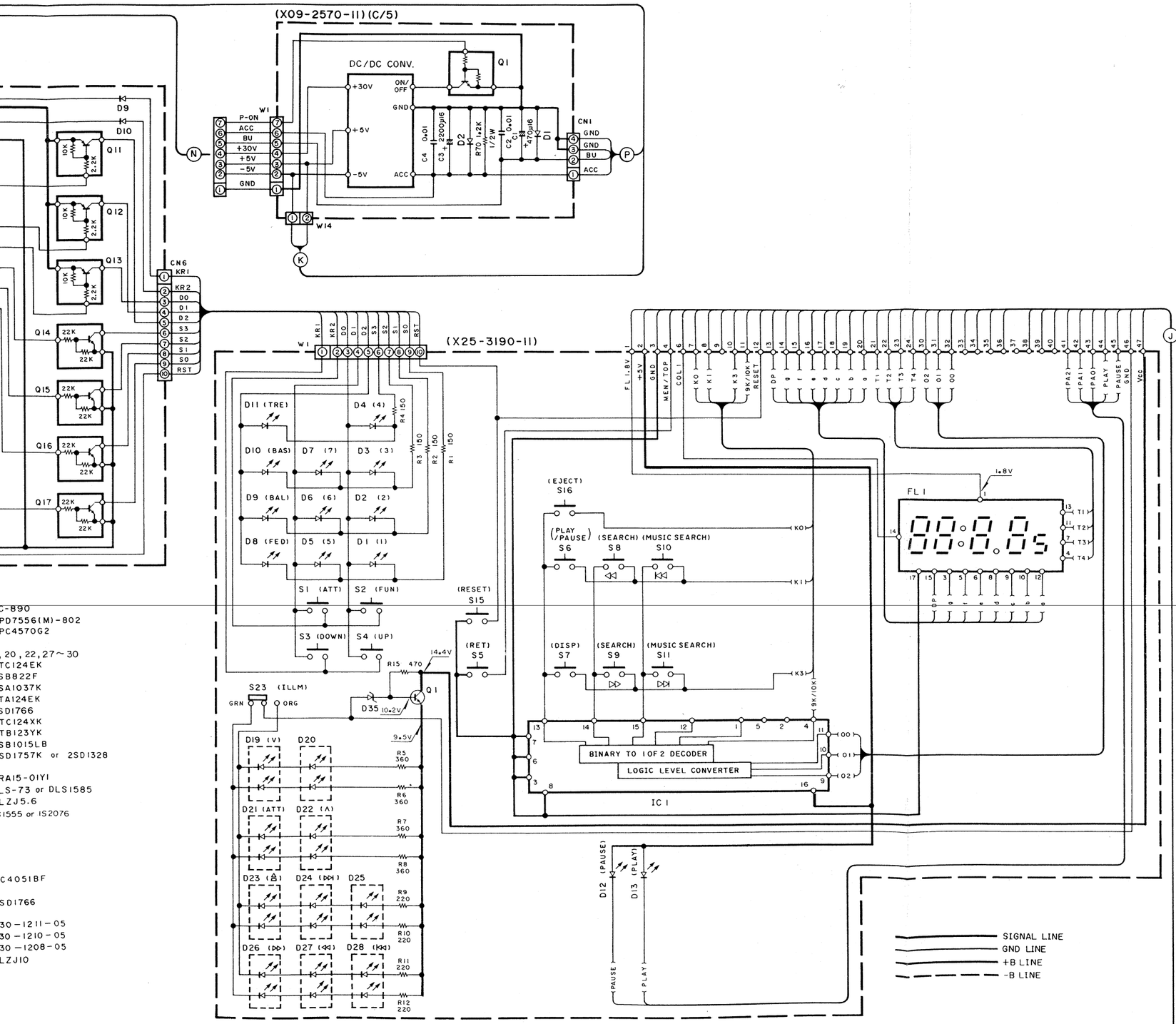


(X09-2570-11)

IC1	: KC-890
IC3	: μPD7556(M)-802
IC4,5	: μPC4570G2
Q2,3,5,14~17,20,22,27~30	: DTC124EK
Q4	: 2SB822F
Q6	: 2SA1037K
Q7,9,18,19	: DTA124EK
Q8	: 2SD1766
Q10	: DTC124XK
Q11~13	: DTB123YK
Q21	: 2SB1015LB
Q23~26	: 2SD1757K or 2SD1328
D5,16	: ERA15-01YI
D6,9,10,13	: RLS-73 or DLS1585
D7,8	: RLZJ5.6
D14	: 1S1555 or 1S2076

(X25-3190-11)

IC1	: TC4051BF
Q1	: 2SD1766
D1~3,5~7	: B30-1211-05
D4,8~13	: B30-1210-05
D19~28	: B30-1208-05
D35	: RLZJ10



C-890
PD7556(M)-802
PC4570G2

20, 22, 27~30
TC124EK
SB822F
SA1037K
TA124EK
SD1766
TC124XK
TB123YK
SB1015LB
SD1757K or 2SD1328

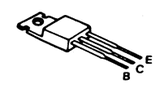
RA15-01Y1
LS-73 or DLS1585
LZJ5.6
1555 or IS2076

C4051BF

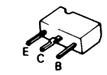
SD1766

30-1211-05
30-1210-05
30-1208-05
LZJ10

2SB1015LB



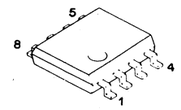
2SB822F



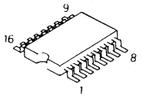
DTA124EK
DTB123YK
DTC124EK
DTC124XK
2SA1037K
2SD1328
2SD1757K

2SD1766

UPC4570G2



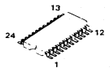
TC4051BF



KC-880A

KC-890

μPD7556(M)-820



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DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

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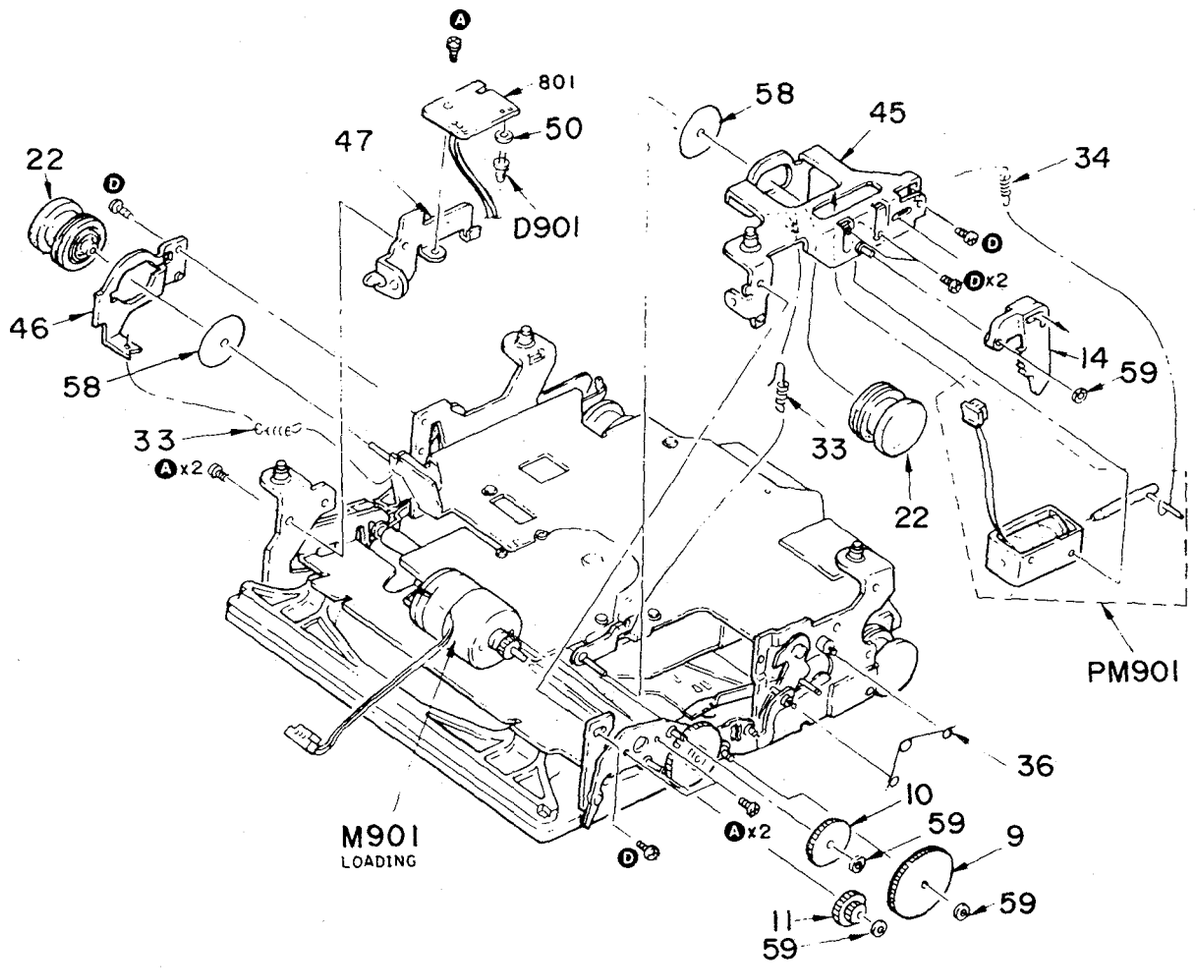
Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen Spannungsmesser gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen Instrumenten oder Geräten u.U. geringfügig.

KDC-80 (K)(2/2)

KDC-80
KENWOOD

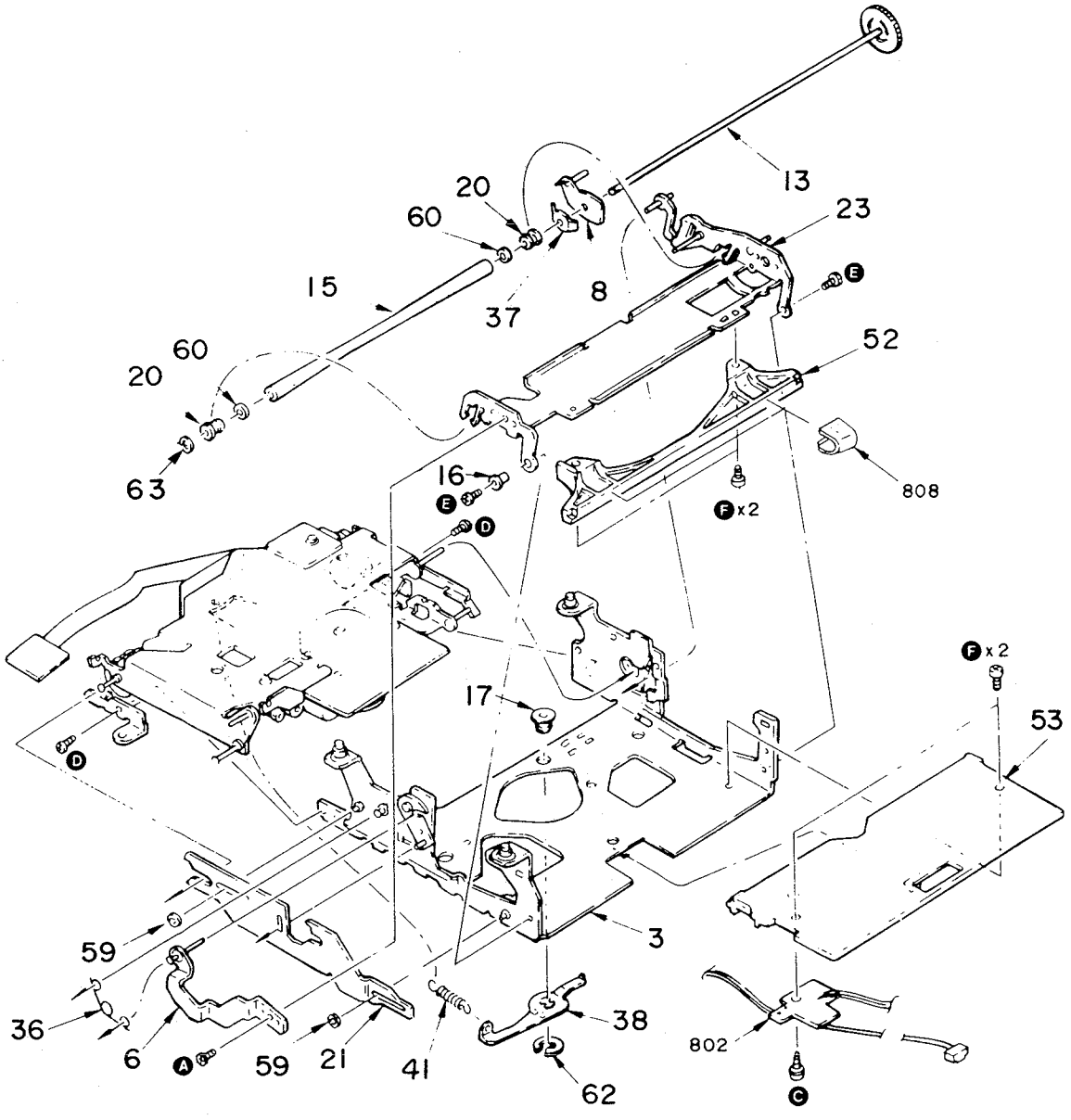
EXPLODED VIEW (MECHANISM)



Ⓐ M2x4	: N09-1299-05
Ⓓ M2x2.2	: N09-1937-05

Parts with the exploded numbers larger than 700 are not supplied.

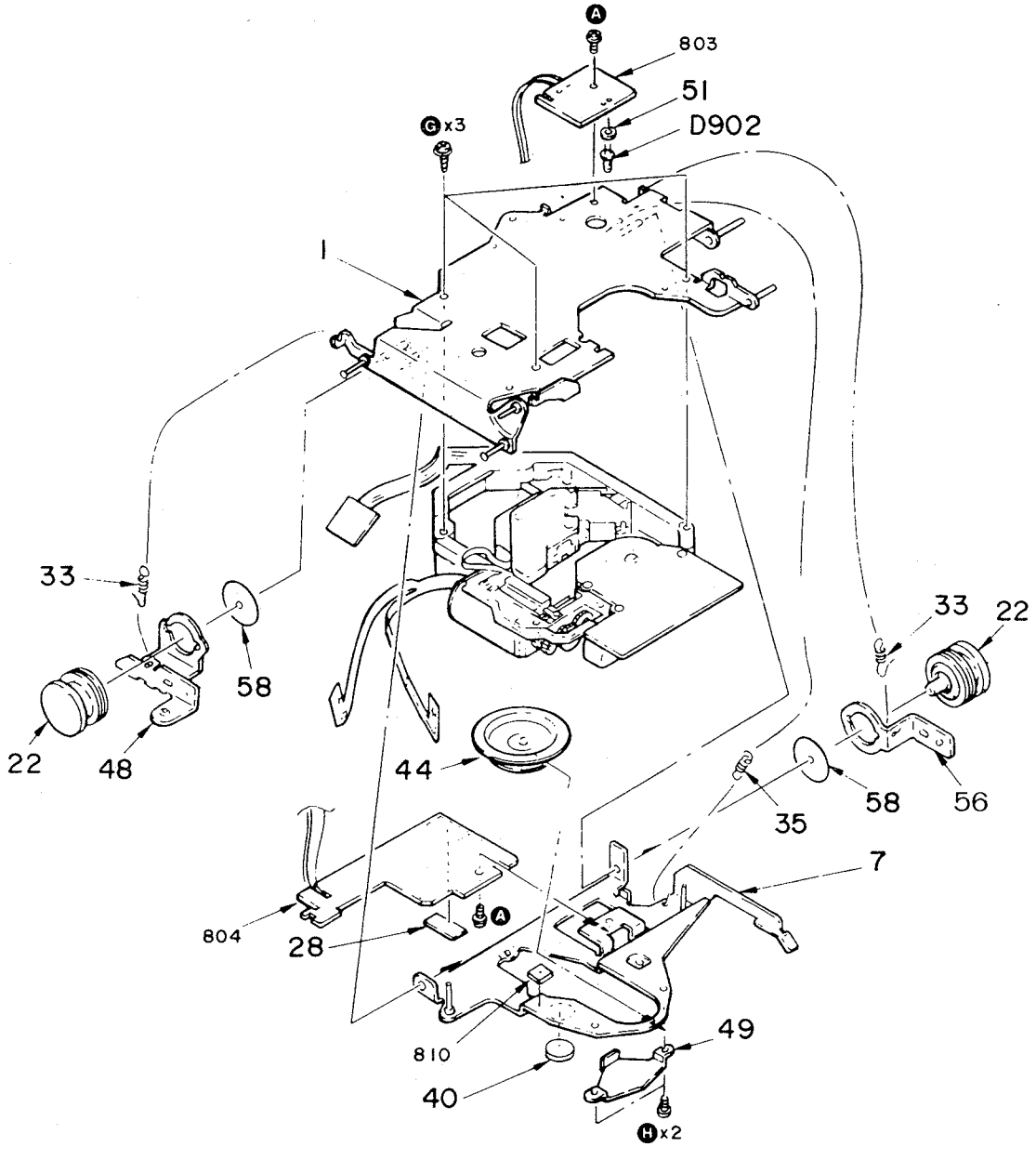
EXPLODED VIEW (MECHANISM)



A	M2x4	: N09 - 1299 - 05
C	M2x5	: N09 - 1936 - 08
D	M2x2.2	: N09 - 1937 - 08
E	M2x5	: N09 - 1938 - 08
F	M2x4	: N09 - 1939 - 08

Parts with the exploded numbers larger than 700 are not supplied.

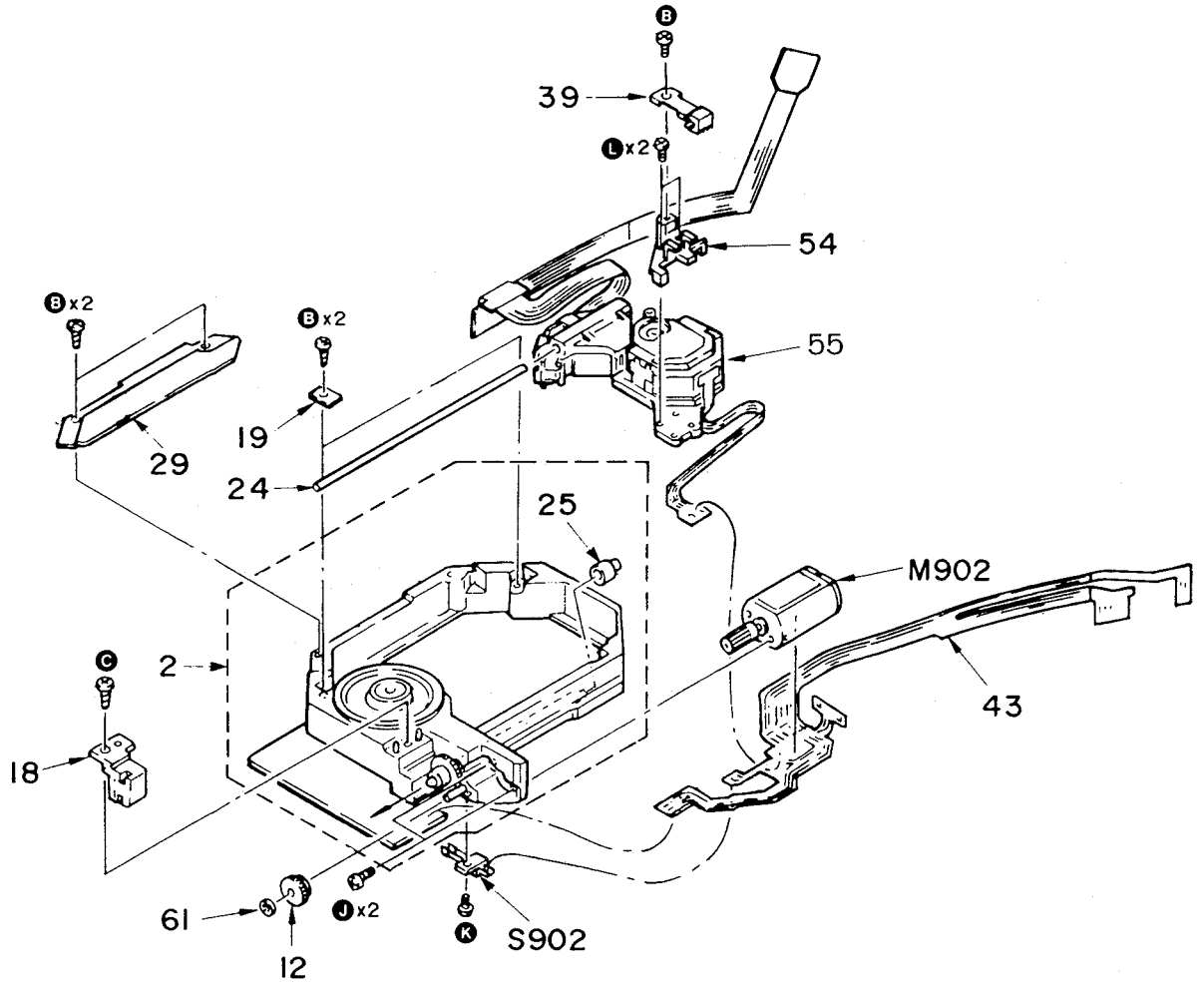
EXPLODED VIEW (MECHANISM)



A M2x4	: N09 - 1299 - 05
G M2x5	: N09 - 1940 - 08
H M1.7x1.6	: N09 - 1941 - 08

Parts with the exploded numbers larger than 700 are not supplied.

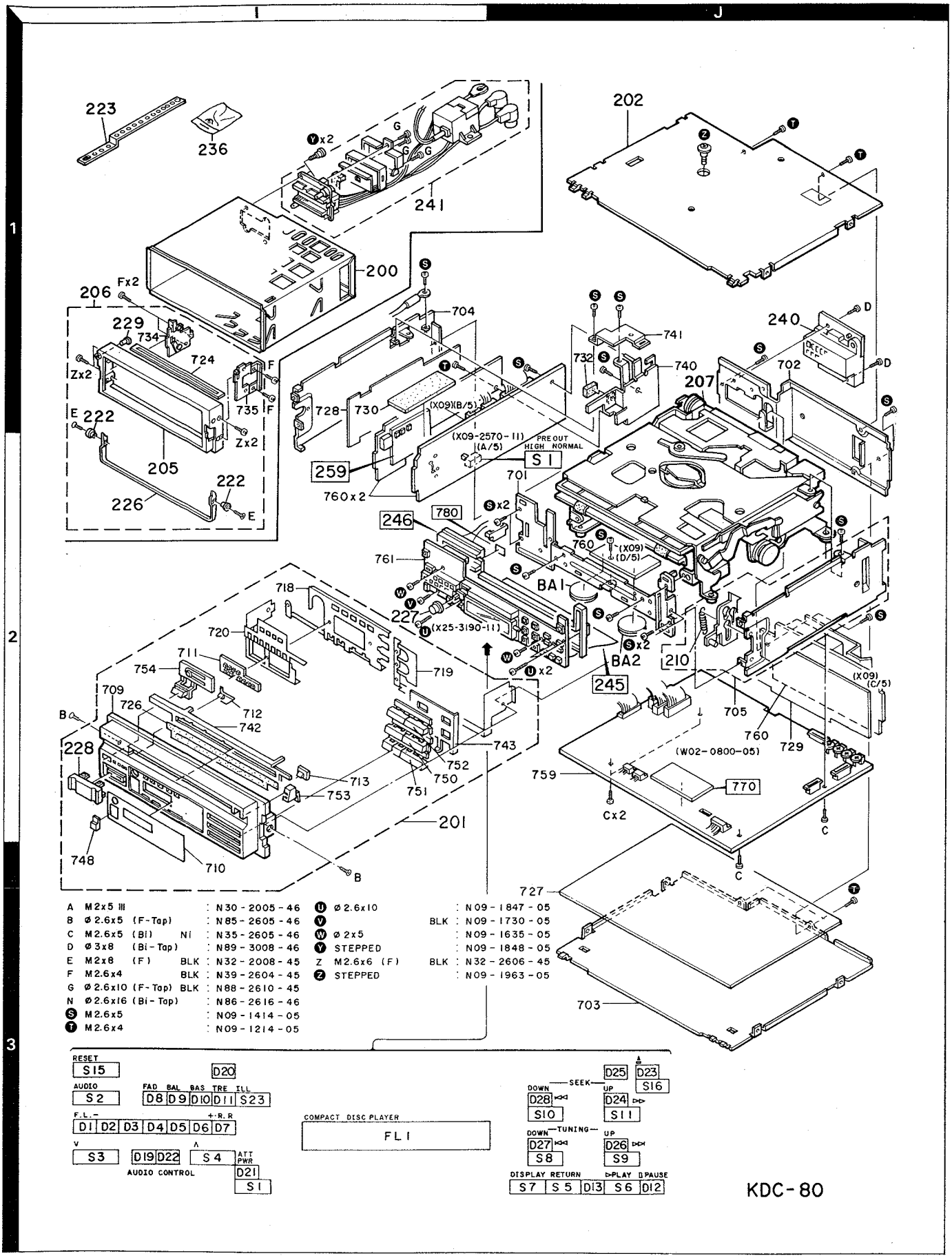
EXPLODED VIEW (MECHANISM)



B M2x4	:	N09-1304-05
C M2x5	:	N09-1936-08
J M2x3	:	N09-1942-08
K M1.4x3	:	N09-1943-08
L M1.7x4	:	N09-1944-08

Parts with the exploded numbers larger than 700 are not supplied.

EXPLODED VIEW (UNIT)



A	M2x5 III		: N30-2005-46	U	Ø2.6x10		: N09-1847-05
B	Ø2.6x5 (F-Tap)		: N85-2605-46	V		BLK	: N09-1730-05
C	M2.6x5 (Bi)	Ni	: N35-2605-46	W	Ø2x5		: N09-1635-05
D	Ø3x8 (Bi-Tap)		: N89-3008-46	Y	STEPPED		: N09-1848-05
E	M2x8 (F)	BLK	: N32-2008-45	Z	M2.6x6 (F)	BLK	: N32-2606-45
F	M2.6x4	BLK	: N39-2604-45	Z	STEPPED		: N09-1963-05
G	Ø2.6x10 (F-Tap)	BLK	: N88-2610-45				
N	Ø2.6x16 (Bi-Tap)		: N86-2616-46				
S	M2.6x5		: N09-1414-05				
T	M2.6x4		: N09-1214-05				

KDC-80

Parts with the exploded numbers larger than 700 are not supplied.

PARTS LIST

* New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
KDC-80						
200	1I	*	A01-1563-11	METALLIC CABINET		
201	2I	*	A20-5420-12	PANEL ASSY		
202	1J	*	A52-0112-03	TOP COVER		
205	2I		B07-1785-01	ESCUTCHEON		
206	1I	*	B07-1786-03	ESCUTCHEON ASSY		
-			B46-0100-10	WARRANTY CARD		
-			B46-0172-03	QUESTIONNAIRE CARD	K	
-		*	B50-8640-00	INSTRUCTION MANUAL(ENG,FRE)	K	
-		*	B50-8641-00	INSTRUCTION MANUAL(E,F,G,D,I)	ET	
-			B58-0860-04	CAUTION CARD		
207	1J		D40-0597-05	MECHANISM ASSY		
210	2J		G01-2040-04	EXTENSION SPRING		
-		*	H01-7732-14	ITEM CARTON CASE		
-		*	H03-0990-14	OUTER CARTON CASE	K	
-		*	H03-0991-14	OUTER CARTON CASE	ET	
-		*	H10-3530-13	POLYSTYRENE FOAMED FIXTURE		
-		*	H10-3566-13	POLYSTYRENE FOAMED FIXTURE		
-		*	H12-2021-14	PACKING FIXTURE		
-		*	H21-0250-04	PROTECTION SHEET		
-		*	H21-0252-04	PROTECTION SHEET		
-		*	H21-0253-04	PROTECTION SHEET		
-		*	H21-0254-04	PROTECTION SHEET		
-			H25-0112-04	PROTECTION BAG (180X250X0.05)		
-			H25-0268-04	PROTECTION BAG		
222	1I,1J		J31-0812-14	COLLAR		
223	1J		J54-0059-04	STAY		
226	2I	*	K01-0084-13	HANDLE		
227	2I		K29-2897-04	KNOB		
228	2I		K29-2889-03	KNOB (BUTTON)AUDIO CONTROL		
229	1I		K27-1752-14	KNOB (BUTTON)		
236	1J		N99-0099-05	SCREW SET		
S	1J,2J		N09-1414-05	TAPTITE SCREW (M2.6X5)		
T	1J,3J		N09-1214-05	TAPTITE SCREW (M2.6X4)		
U	1I,1J		N09-1847-05	EVATITE SCREW (2.6X10)		
V	2I		N09-1730-05	TAPPING SCREW		
Y	1I		N09-1848-05	STEPPED SCREW		
Z	1J		N09-1963-05	SCREW		
BA1 ,2	2J		W09-0064-05	BATTERY (LITHIUM)		
240	1J	*	X90-2690-10	COMPOUND ASSY UNIT(26P CASE)		
241	1I	*	X90-2700-10	COMPOUND ASSY UNIT(26P CORD)		
MOTHER UNIT (W02-0800-05)						
C101			CK41DB1H221K	CYLND CHIP C 220PF K		
C102			C90-0508-05	ELECTRO 2.2UF 50WV		
C103			CC41DSL1H560J	CYLND CHIP C 56PF J		
C104		*	CK73EB1H182K	CHIP C 1800PF K		
C105,106			CK41DB1H101K	CYLND CHIP C 100PF K		
C107		*	CC41DSL1H200J	CYLND CHIP C 20PF J		
C108			CK41DB1H101K	CYLND CHIP C 100PF K		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

⚠ indicates safety critical components.

PARTS LIST

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Telle ohne **Parts No.** werden nicht gellefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格			Destination 仕向	Remarks 備考
C116			CK73EB1H102K	CHIP C	1000PF	K		
C125			CK45B1H101K	CERAMIC	100PF	K		
C128			CC41DSL1H470J	CYLND CHIP C	47PF	J		
C201			CK41DB1H221K	CYLND CHIP C	220PF	K		
C202			C90-0508-05	ELECTRO	2.2UF	50WV		
C203			CC41DSL1H560J	CYLND CHIP C	56PF	J		
C204		*	CK73EB1H182K	CHIP C	1800PF	K		
C205,206			CK41DB1H101K	CYLND CHIP C	100PF	K		
C207		*	CC41DSL1H200J	CYLND CHIP C	20PF	J		
C208			CK41DB1H101K	CYLND CHIP C	100PF	K		
C216			CK73EB1H102K	CHIP C	1000PF	K		
C225			CK45B1H101K	CERAMIC	100PF	K		
C228			CC41DSL1H470J	CYLND CHIP C	47PF	J		
C301-304			C90-0495-05	ELECTRO	47UF	6.3WV		
C309,310			C90-0495-05	ELECTRO	47UF	6.3WV		
C313,314			CE04DW0J331M	ELECTRO	330UF	6.3WV		
C315,316			CK73EB1H223K	CHIP C	0.022UF	K		
C501			CF92V1H333J	MF	0.033UF	J		
C502,503			CF92V1H103J	MF	0.010UF	J		
C505		*	C90-1644-08	ELECTRO	56UF	6.3WV		
C506			CF92V1H333J	MF	0.033UF	J		
C507			C90-0495-05	ELECTRO	47UF	6.3WV		
C508			C90-0484-05	ELECTRO	0.47UF	50WV		
C509			CF92V1H103J	MF	0.010UF	J		
C510		*	C90-1644-08	ELECTRO	56UF	6.3WV		
C511			C90-0495-05	ELECTRO	47UF	6.3WV		
C512-514			CF92V1H104J	MF	0.10UF	J		
C515			CS15E1C3R3M	TANTAL	3.3UF	16WV		
C516			C90-0495-05	ELECTRO	47UF	6.3WV		
C517			CF92V1H104J	MF	0.10UF	J		
C519			CF92V1H104J	MF	0.10UF	J		
C520		*	CK45SL1H100J	CERAMIC	10PF	J		
C521			CF92V1H683J	MF	0.068UF	J		
C522-525		*	CE04DW0J470M	ELECTRO	47UF	6.3WV		
C526			C90-0481-05	ELECTRO	3.3UF	50WV		
C527			C90-0497-05	ELECTRO	22UF	10WV		
C528,529			C90-0495-05	ELECTRO	47UF	6.3WV		
C530			CK45B1H102K	CERAMIC	1000PF	K		
C531			C90-0484-05	ELECTRO	0.47UF	50WV		
C532			CF92V1H333J	MF	0.033UF	J		
C533			CQ92FM1H222J	MYLAR	2200PF	J		
C534			CF92V1H183J	MF	0.018UF	J		
C535			CK73EB1H102K	CHIP C	1000PF	K		
C536			C90-0495-05	ELECTRO	47UF	6.3WV		
C537			CK73EF1E334Z	CHIP C	0.33UF	Z		
C538			CQ92FM1H472J	MYLAR	4700PF	J		
C539,540			C90-0824-05	ELECTRO	1UF	50WV		
C541,542		*	CC41DSL1H120J	CYLND CHIP C	12PF	J		
C543			C90-0831-05	ELECTRO	33UF	10WV		
C545			C90-0831-05	ELECTRO	33UF	10WV		
C546			C90-0496-05	ELECTRO	100UF	6.3WV		
C547,548		*	CC41DSL1H120J	CYLND CHIP C	12PF	J		
C550			C90-0481-05	ELECTRO	3.3UF	50WV		
C551			CE04DW1V221M	ELECTRO	220UF	35WV		
C552			C90-0495-05	ELECTRO	47UF	6.3WV		

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C553			CK73EB1H102K	CHIP C 1000PF K		
C554,555			C90-0495-05	ELECTRO 47UF 6.3WV		
C556			CK41DB1H151K	CYLND CHIP C 150PF K		
C557			CK73EB1E104K	CHIP C 0.10UF K		
C558			C90-0497-05	ELECTRO 22UF 10WV		
C559			C90-0482-05	ELECTRO 4.7UF 25WV		
C560			C90-0478-05	ELECTRO 10UF 16WV		
C562,563			CE04DW0J331M	ELECTRO 330UF 6.3WV		
C564,565			CE04DW0J331M	ELECTRO 330UF 6.3WV		
C566			C90-0495-05	ELECTRO 47UF 6.3WV		
C567			CK73EB1E104K	CHIP C 0.10UF K		
C568			C90-0822-05	ELECTRO 47UF 16WV		
C569		*	CK45DB1H221K	CERAMIC 220PF K		
C570			CK73EB1E104K	CHIP C 0.10UF K		
C572		*	CC41DSL1H200J	CYLND CHIP C 20PF J		
C574-577			CK73EB1E104K	CHIP C 0.10UF K		
C578			CK73EB1H103K	CHIP C 0.010UF K		
C579			CK73EB1H102K	CHIP C 1000PF K		
C580-582			CK73EB1H223K	CHIP C 0.022UF K		
C583			CS15E1C4R7M	TANTAL 4.7UF 16WV		
C584			CE04CW1H0R1M	ELECTRO 0.1UF 50WV		
C585			CK73EB1H223K	CHIP C 0.022UF K		
C591,592			CK73EB1E104K	CHIP C 0.10UF K		
C594			CK73FF1E104Z	CHIP C 0.10UF Z		
-		*	E10-1213-08	CONNECTOR		
CNP502		*	E10-0815-08	CONNECTOR		
CNP503		*	E10-0410-08	CONNECTOR		
L301,302		*	L39-0163-08	COIL		
L501		*	L39-0164-08	COIL		
L502		*	L39-0162-08	COIL		
L503,504		*	L39-0163-08	COIL		
T501		*	L19-0058-08	BALUN TRANSFORMER		
X501		*	L77-1133-08	CRYSTAL RESONATOR		
X502		*	L77-1134-08	CRYSTAL RESONATOR		
JW501-506			R92-0338-05	CLYND CHIP R 0 OHM		
R101			RD41DB2B472J	CYLND CHIP R 4.7K J 1/8W		
R102			RD41DB2B183J	CYLND CHIP R 18K J 1/8W		
R103,104			RD41DB2B822J	CYLND CHIP R 8.2K J 1/8W		
R105,106			RD41DB2B203J	CYLND CHIP R 20K J 1/8W		
R108		*	RD41DB2B912J	CYLND CHIP R 9.1K J 1/8W		
R109,110			RD41DB2B183J	CYLND CHIP R 18K J 1/8W		
R111		*	RD41DB2B912J	CYLND CHIP R 9.1K J 1/8W		
R112			RD41DB2B563J	CYLND CHIP R 56K J 1/8W		
R113			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R114			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R131			RD41DB2B563J	CYLND CHIP R 56K J 1/8W		
R201			RD41DB2B472J	CYLND CHIP R 4.7K J 1/8W		
R202			RD41DB2B183J	CYLND CHIP R 18K J 1/8W		
R203,204			RD41DB2B822J	CYLND CHIP R 8.2K J 1/8W		
R205,206			RD41DB2B203J	CYLND CHIP R 20K J 1/8W		
R208		*	RD41DB2B912J	CYLND CHIP R 9.1K J 1/8W		
R209,210			RD41DB2B183J	CYLND CHIP R 18K J 1/8W		
R211		*	RD41DB2B912J	CYLND CHIP R 9.1K J 1/8W		
R212			RD41DB2B563J	CYLND CHIP R 56K J 1/8W		

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R213			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R214			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R231			RD41DB2B563J	CYLND CHIP R 56K J 1/8W		
R301			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R303,304			RD41DB2B472J	CYLND CHIP R 4.7K J 1/8W		
R501		*	RD41DB2B203J	CYLND CHIP R 20K J 1/8W		
R503			RD41DB2B133J	CYLND CHIP R 13K J 1/8W		
R504			RD41DB2B222J	CYLND CHIP R 2.2K J 1/8W		
R505		*	RD41DB2B620J	CYLND CHIP R 62 J 1/8W		
R506			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R507			RD41DB2B750J	CYLND CHIP R 75 J 1/8W		
R508			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R509			RD41DB2B104J	CYLND CHIP R 100K J 1/8W		
R510		*	RD41DB2B113J	CYLND CHIP R 11K J 1/8W		
R511		*	RD41DB2B164J	CYLND CHIP R 160K J 1/8W		
R512			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R513			RD41DB2B474J	CYLND CHIP R 470K J 1/8W		
R514			RD41DB2B823J	CYLND CHIP R 82K J 1/8W		
R515			RD41DB2B563J	CYLND CHIP R 56K J 1/8W		
R516			RD41DB2B823J	CYLND CHIP R 82K J 1/8W		
R517			RD41DB2B124J	CYLND CHIP R 120K J 1/8W		
R518			RD41DB2B153J	CYLND CHIP R 15K J 1/8W		
R519			RD41DB2B822J	CYLND CHIP R 8.2K J 1/8W		
R520			RD41DB2B514J	CYLND CHIP R 510K J 1/8W		
R521			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R522			RD41DB2B683J	CYLND CHIP R 68K J 1/8W		
R523			RD41DB2B332J	CYLND CHIP R 3.3K J 1/8W		
R524			RD41DB2B203J	CYLND CHIP R 20K J 1/8W		
R525			RD41DB2B105J	CYLND CHIP R 1.0M J 1/8W		
R526-529			RD41DB2B1R0J	CYLND CHIP R 1.0 J 1/8W		
R530			RD41DB2B474J	CYLND CHIP R 470K J 1/8W		
R531			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R533			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R534			RD41DB2B104J	CYLND CHIP R 100K J 1/8W		
R535			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R536			RD41DB2B104J	CYLND CHIP R 100K J 1/8W		
R537,538			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R540,541			RD41DB2B181J	CYLND CHIP R 180 J 1/8W		
R542			RD41DB2B243J	CYLND CHIP R 24K J 1/8W		
R543			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R544			RD41DB2B471J	CYLND CHIP R 470 J 1/8W		
R545			RD41DB2B511J	CYLND CHIP R 510 J 1/8W		
R546			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R547			RD41DB2B223J	CYLND CHIP R 22K J 1/8W		
R548			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R549			RD41DB2B223J	CYLND CHIP R 22K J 1/8W		
R550			RD41DB2B100J	CYLND CHIP R 10 J 1/8W		
R551			RD41DB2B223J	CYLND CHIP R 22K J 1/8W		
R552			RD41DB2B473J	CYLND CHIP R 47K J 1/8W		
R553			RD41DB2B332J	CYLND CHIP R 3.3K J 1/8W		
R554			RD41DB2B330J	CYLND CHIP R 33 J 1/8W		
R555			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R556			RD41DB2B223J	CYLND CHIP R 22K J 1/8W		
R557			RD41DB2B104J	CYLND CHIP R 100K J 1/8W		
R558			RD41DB2B622J	CYLND CHIP R 6.2K J 1/8W		

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R559			RD41DB2B473J	CYLND CHIP R 47K J 1/8W		
R560-567			RD41DB2B181J	CYLND CHIP R 180 J 1/8W		
R568,569			RD41DB2B100J	CYLND CHIP R 10 J 1/8W		
R570			RD41DB2B560J	CYLND CHIP R 56 J 1/8W		
R571			RD41DB2B680J	CYLND CHIP R 68 J 1/8W		
R572			RD41DB2B101J	CYLND CHIP R 100 J 1/8W		
R574			RD41DB2B472J	CYLND CHIP R 4.7K J 1/8W		
R575			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R576		*	RD41DB2B910J	CYLND CHIP R 91 J 1/8W		
R578			RD41DB2B822J	CYLND CHIP R 8.2K J 1/8W		
R579			RD41DB2B272J	CYLND CHIP R 2.7K J 1/8W		
R580			RD41DB2B622J	CYLND CHIP R 6.2K J 1/8W		
R581			RD41DB2B223J	CYLND CHIP R 22K J 1/8W		
R582			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R583			RD41DB2B153J	CYLND CHIP R 15K J 1/8W		
R585			RD41DB2B393J	CYLND CHIP R 39K J 1/8W		
R590			RD41DB2B105J	CYLND CHIP R 1.0M J 1/8W		
R591			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
RV501-504			R12-3072-05	POTENTIOMETER(22KB)T/F OFST,GA		
RV505			R12-1105-08	POTENTIOMETER(2.2KB)VCO		
D502,503		*	DSC010	DIODE		
D504		*	V06C	DIODE		
D504			10E2	DIODE		
D505			RD5.6E(B3)	ZENER DIODE		
D506			1SS106	DIODE		
D507		*	DSC010	DIODE		
D508,509		*	DCA015	DIODE		
D510		*	RD7.5ES(B)	ZENER DIODE		
IC101,102		*	M5203FP	IC(OP AMP X2)		
IC201,202		*	M5203FP	IC(OP AMP X2)		
IC301		*	PCM55HP-S	IC(DA CONVERTER)		
IC302,303			TC4053BF	IC(3-INPUT 2CH MPX/DE-MPX)		
IC501		*	CXA1081Q	IC(SURVO SIGNAL PROCESSOR)		
IC502			CXA1082AQ	IC(SERVO SIGNAL PROCESSOR)		
IC503			CXD1130Q	IC(DIGITAL SIGNAL PROCESSOR)		
IC504		*	L272M	IC(MOTOR DRIVE)		
IC505		*	MB88505H-530M	IC(MICROPROCESSOR)		
IC506		*	MB88505PF-G-613	IC(MICROPROCESSOR)		
IC507		*	CXK5816	IC(2KX8 RAM)		
IC507		*	LC3516AML-15	IC(2KX8 RAM)		
IC508		*	M54940FP	IC(FLUORESCENT DRIVE/DECODER)		
IC509		*	UPD82C43G	IC(MICROPROCESSOR)		
IC510		*	LC74HC365M	IC(3 STATE BUFFER)		
IC512		*	MB88201-534M	IC(I/O CONTROL)		
IC513			LC74HC04M	IC(HEX INVERTER)		
IC513			TC74HC04F	IC(HEX INVERTER)		
IC514-516			S-8054HN	IC(VOLTAGE DETECTOR)		
Q501		*	2SD1623	TRANSISTOR		
Q502		*	2SB1123	TRANSISTOR		
Q503		*	2SD1623	TRANSISTOR		
Q504		*	2SB1123	TRANSISTOR		
Q505		*	2SA1179	TRANSISTOR		
Q505			2SA812	TRANSISTOR		
Q506		*	2SB1123	TRANSISTOR		
Q507			2SC2712	TRANSISTOR		

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Q507			2SC2812	TRANSISTOR		
Q508,509		*	2SA1344	TRANSISTOR		
Q510		*	2SC3395	TRANSISTOR		
Q511		*	2SC3398	TRANSISTOR		
Q512-515		*	2SA1179	TRANSISTOR		
Q512-515			2SA812	TRANSISTOR		
Q516		*	2SD1623(R)	TRANSISTOR		
Q517		*	2SA1179	TRANSISTOR		
Q517			2SA812	TRANSISTOR		
Q518-520			2SC2712	TRANSISTOR		
Q518-520			2SC2812	TRANSISTOR		
Q522		*	2SC3395	TRANSISTOR		
Q523			DTB123YK	DIGITAL TRANSISTOR		
Q524		*	2SC3398	TRANSISTOR		
Q525			DTB123YK	DIGITAL TRANSISTOR		
Q526		*	2SC2712	TRANSISTOR		
Q526		*	2SC2812	TRANSISTOR		
Q528,529		*	2SC3398	TRANSISTOR		
Q530-532		*	2SC3398	TRANSISTOR		
Q533		*	DTA114WK	DIGITAL TRANSISTOR		
Q534		*	2SC3398	TRANSISTOR		
Q536,537		*	DTB113EK	DIGITAL TRANSISTOR		
Q538,539		*	DTD113ZK	DIGITAL TRANSISTOR		
Q540		*	2SC2712	TRANSISTOR		
Q541		*	2SA1510	TRANSISTOR		
TH501-503		*	ERT-D2FHJ802T	THERMISTER		
AUDIO UNIT (X09-2570-11)						
C1			CE04DW1C471M	ELECTRO 470UF	16WV	
C2			CK73EB1H103K	CHIP C 0.010UF	K	
C3			C90-1401-05	ELECTRO 2200UF	16WV	
C4			CK73EB1H103K	CHIP C 0.010UF	K	
C5			C90-0478-05	ELECTRO 10UF	16WV	
C6			C90-0477-05	ELECTRO 0.1UF	50WV	
C7			C90-1263-05	ELECTRO 100UF	16WV	
C8			CE04DW1C102M	ELECTRO 1000UF	16WV	
C11			CK41DF1E223Z	CYLND CHIP C 0.022UF	Z	
C12			C90-0824-05	ELECTRO 1UF	50WV	
C13 ,14			C90-0495-05	ELECTRO 47UF	6.3WV	
C19 -22			CC41DSL1H330J	CYLND CHIP C 33PF	J	
C23 -26			CE04MW1C100M	ELECTRO 10UF	16WV	
C30			CE04CW0J101M	ELECTRO 100UF	6.3WV	
C31			CE04CW1C100M	ELECTRO 10UF	16WV	
J1 -27			R92-0338-05	CLYND CHIP R 0 OHM		
J31			R92-0338-05	CLYND CHIP R 0 OHM		
J51 -57			R92-0670-05	CHIP R 0 OHM		
R1			RK73FB2A473J	CHIP R 47K	J 1/10W	
R2			RK73FB2A103J	CHIP R 10K	J 1/10W	
R3			RK73FB2A223J	CHIP R 22K	J 1/10W	
R4			RK73FB2A103J	CHIP R 10K	J 1/10W	
R5			RK73FB2A102J	CHIP R 1.0K	J 1/10W	
R7			RD14DB2H102J	SMALL-RD 1.0K	J 1/2W	
R8			RK73FB2A223J	CHIP R 22K	J 1/10W	
R9			RD14DB2H561J	SMALL-RD 560	J 1/2W	
R13			RD14DB2H470J	SMALL-RD 47	J 1/2W	

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R14			RD41DB2B472J	CYLND CHIP R 4.7K J 1/8W		
R15			RD41DB2B102J	CYLND CHIP R 1.0K J 1/8W		
R22 ,23			RD41DB2B563J	CYLND CHIP R 56K J 1/8W		
R24			RD41DB2B681J	CYLND CHIP R 680 J 1/8W		
R25 ,26			RD41DB2B222J	CYLND CHIP R 2.2K J 1/8W		
R27			RK73FB2A103J	CHIP R 10K J 1/10W		
R28			RD14DB2H330J	SMALL-RD 33 J 1/2W		
R29 ,30			RD41DB2B362J	CYLND CHIP R 3.6K J 1/8W		
R31 -34			RD41DB2B122J	CYLND CHIP R 1.2K J 1/8W		
R35 -38			RD41DB2B392J	CYLND CHIP R 3.9K J 1/8W		
R39 -42			RD41DB2B561J	CYLND CHIP R 560 J 1/8W		
R43 -46			RD41DB2B473J	CYLND CHIP R 47K J 1/8W		
R47 -50			RD41DB2B163J	CYLND CHIP R 16K J 1/8W		
R51 -54		*	RD41DB2B134J	CYLND CHIP R 130K J 1/8W		
R55 -58			RD41DB2B473J	CYLND CHIP R 47K J 1/8W		
R59 -62			RD41DB2B273J	CYLND CHIP R 27K J 1/8W		
R63 ,64			RD41DB2B100J	CYLND CHIP R 10 J 1/8W		
R65			RD41DB2B104J	CYLND CHIP R 100K J 1/8W		
R66			RD41DB2B223J	CYLND CHIP R 22K J 1/8W		
R67			RD41DB2B753J	CYLND CHIP R 75K J 1/8W		
R68			RD41DB2B560J	CYLND CHIP R 56 J 1/8W		
R69			RD41DB2B103J	CYLND CHIP R 10K J 1/8W		
R70		*	RD14DB2H122J	SMALL-RD 1.2K J 1/2W		
S1	2J		S31-1011-05	SLIDE SWITCH (OPEN/CLOSE)		
D1 ,2			ERA15-01Y1	DIODE		
D5			ERA15-01Y1	DIODE		
D6			DLS1585	DIODE		
D6			RLS-73	DIODE		
D7 ,8			RLZJ5.6	ZENER DIODE		
D9 ,10			DLS1585	DIODE		
D9 ,10			RLS-73	DIODE		
D13			DLS1585	DIODE		
D13			RLS-73	DIODE		
D14			1S1555	DIODE		
D14			1S2076	DIODE		
D15			DLS1585	DIODE		
D15			RLS-73	DIODE		
D16			ERA15-01Y1	DIODE		
IC1		*	KC-890	IC(VOLUME CONTROL)		
IC3		*	UPD7556G(M)-802	IC(MICROPROCESSOR)		
IC4 ,5			UPC4570G2	IC(OP AMP X2)		
Q1 -3			DTC124EK	DIGITAL TRANSISTOR		
Q4			2SB822F	TRANSISTOR		
Q5			DTC124EK	DIGITAL TRANSISTOR		
Q6			2SA1037K	TRANSISTOR		
Q7			DTA124EK	DIGITAL TRANSISTOR		
Q8			2SD1766	TRANSISTOR		
Q9			DTA124EK	DIGITAL TRANSISTOR		
Q10			DTC124XK	DIGITAL TRANSISTOR		
Q11 -13			DTB123YK	DIGITAL TRANSISTOR		
Q14 -17			DTC124EK	DIGITAL TRANSISTOR		
Q18 ,19			DTA124EK	DIGITAL TRANSISTOR		
Q20			DTC124EK	DIGITAL TRANSISTOR		
Q21			2SB1015LB	TRANSISTOR		

E: Scandinavia & Europe **K**: USA **P**: Canada
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PARTS LIST

* New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
Q22			DTC124EK	DIGITAL TRANSISTOR		
Q23 -26			2SD1328	TRANSISTOR		
Q23 -26			2SD1757K	TRANSISTOR		
Q27 -30			DTC124EK	DIGITAL TRANSISTOR		
Q31			2SA1036K	TRANSISTOR		
259	1I	*	W02-0794-15	ELECTRIC CIRCUIT MODULE		
SWITCH UNIT (X25-3190-11)						
D1 -3	3I	*	B30-1211-05	LED (FL,-)		
D4	3I	*	B30-1210-05	LED		
D5 -7	3I	*	B30-1211-05	LED (R,R)		
D8 -13	3I,3J	*	B30-1210-05	LED (TONE,FM,AM)		
D19 -28	3I,3J	*	B30-1208-05	LED (ATT,TUNING)		
245	2J	*	J25-5785-03	PRINTED WIRING BOARD		
246	2I	*	J19-2928-02	HOLDER		
W	2I,2J		N09-1635-05	TAPTITE SCREW (Ø2X5)		
R1 -4			RD41DB2B151J	CYLND CHIP R 150 J 1/8W		
R5 -8			RD41DB2B361J	CYLND CHIP R 360 J 1/8W		
R9 -12			RD41DB2B221J	CYLND CHIP R 220 J 1/8W		
R15			RD41DB2B471J	CYLND CHIP R 470 J 1/8W		
S1 -11	3I,3J		S40-1096-05	PUSH SWITCH (ATT,AUDIO)		
S15 ,16	3I,3J	*	S40-1117-05	PUSH SWITCH (PRESET,EJECT)		
S23	3I	*	S40-2365-05	PUSH SWITCH (ILL)		
D35			RLZJ10	ZENER DIODE		
FL1	3I	*	FV029P1	FLUORESCENT INDICATOR TUBE		
IC1		*	TC4051BF	IC(8CH MPX/ DE-MPX)		
Q1			2SD1766	TRANSISTOR		
SCREW SET (N99-0099-05)						
-			N09-0335-05	SCREW (Ø5X16) X1		
-			N09-0366-05	HEXAGON BOLT (M5X20) X2		
-			N10-1050-46	HEXAGON NUT (M5) X2		
-			N14-0117-05	FLANGE NUT (M5) X1		
MECHANISM ASS'Y (D40-0597-05)						
1	1E	*	A11-0260-08	SUB CHASSIS ASSY		
2	2G	*	A13-1103-08	FRAME		
3	3D	*	A13-1104-08	FRAME ASSY (S2) MD		
6	3C	*	D10-2086-08	ARM		
7	2F	*	D10-2087-08	ARM ASSY		
8	2D	*	D10-2088-08	LEVER ASSY		
9	2B	*	D13-0668-08	GEAR (DOWN)		
10	2B	*	D13-0669-08	GEAR (B2)		
11	3B	*	D13-0670-08	GEAR (A2)		
12	2G	*	D13-0671-08	GEAR		
13	1D	*	D13-0672-08	GEAR (ROLLER SHAFT)		
14	2B	*	D13-0673-08	GEAR (RACK)		
15	1C	*	D14-0269-08	ROLLER		
16	2C	*	D21-1435-08	SHAFT (R) ROLLER SHAFT		
17	2C	*	D21-1436-08	SHAFT		
18	2G	*	D23-0232-08	RETAINER		
19	2G	*	D23-0234-08	RETAINER (GUIDE SHAFT)		
20	1C,2C	*	D32-0171-08	STOPPER (BEARING)		
21	3C	*	D32-0172-08	LOCK PLATE		
22	2A,2E	*	D39-0189-08	DAMPER (S)		

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Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
23	1D	*	D10-2085-08	ARM ASSY		
24	2G	*	D21-1437-08	SHAFT		
25	2G	*	D23-0233-08	RETAINERD		
28	3E	*	F20-0936-08	INSULATING SHEET		
29	2G	*	F07-0523-08	COVER		
33	2A,2F	*	G01-2189-08	TENSION SPRING		
34	1B	*	G01-2190-08	TENSION SPRING		
35	2F	*	G01-2192-08	TENSION SPRING		
36	2B,3C	*	G01-2193-08	TORSION COIL SPRING (S)		
37	1C	*	G02-0464-08	FLAT SPRING (S)		
38	3D	*	G02-0465-08	FLAT SPRING		
39	1G	*	G02-0466-08	FLAT SPRING ASSY		
40	2E	*	G11-1249-08	CUSHION		
41	3C	*	G01-2191-08	TENSION SPRING		
43	2H	*	J25-5830-08	PRINTED WIRING BOARD(FPC,MOTOR		
44	3E	*	J11-0114-08	CLAMPER		
45	1B	*	J19-2941-08	BRACKET (B)		
46	2A	*	J19-2942-08	BRACKET (A)		
47	1A	*	J19-2943-08	BRACKET (LED PCB)		
48	2E	*	J19-2944-08	BRACKET		
49	3F	*	J21-5188-08	MOUNTING HARDWARE		
50	1A	*	J30-0239-08	SPACER (LED)		
51	1F	*	J30-0239-08	SPACER		
52	1D	*	J90-0604-08	GUIDE		
53	2D	*	J90-0605-08	GUIDE		
54	2D	*	J90-0606-08	GUIDE		
55	1H	*	J91-0346-08	PICKUP ASSY (KSS-1608)		
56	2F	*	J19-2945-08	LED,LEAD HOLDER,BRACKET ASSY		
58	2A,1B	*	N19-1117-08	FLAT WASHER		
59	2B,2C	*	N19-1118-08	FLAT WASHER (REEL)		
60	1C,2C	*	N19-1119-08	FLAT WASHER		
61	2G	*	N19-1120-08	FLAT WASHER		
62	3D	*	N29-0253-08	FASTENER (Ø5)		
63	2C	*	N29-0254-08	FASTENER (Ø2.2)		
A	1A,3C		N09-1299-05	SCREW (M2X4)		
B	1H		N09-1304-05	SCREW (M2X4)		
C	2G	*	N09-1936-08	SCREW (M2X5)		
D	2B	*	N09-1937-08	SCREW (M2X2.2)		
E	1D	*	N09-1938-08	SCREW (M2X5)		
F	2D	*	N09-1939-08	SCREW (M2X4)		
G	1E	*	N09-1940-08	SCREW (M2X5)		
H	3F	*	N09-1941-08	SCREW (M1.7X1.6)		
J	3G	*	N09-1942-08	SCREW (M2X3) MOTOR		
K	3G	*	N09-1943-08	SCREW (M1.4X3)LEAF SW		
L	1H	*	N09-1944-08	SCREW (M1.7X4)		
S902	3H	*	S46-1107-08	LEAF SWITCH (LIMIT)		
M901	2A	*	T43-0052-08	DD MOTOR ASSY (LOADING)		
M902	2H	*	T43-0053-08	DD MOTOR ASSY (SLED)		
PM901	2B	*	T94-0206-08	SOLENOID		
D901,902	1A,1F		TLR123	LED		

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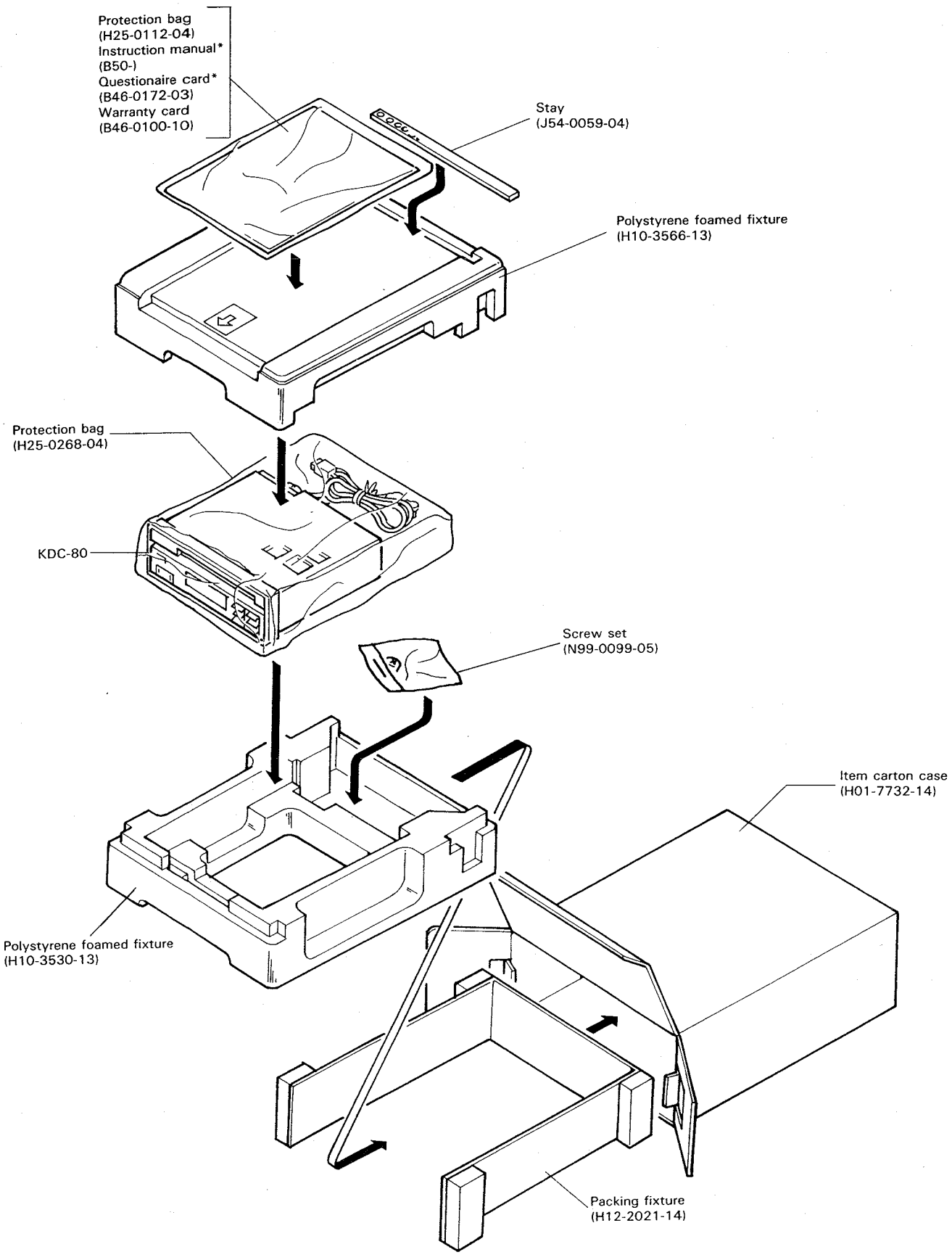
PACKING



* Refer to parts list on page 78.

KDC-80

SPECIFICATIONS

Disc Section

Laser Diode.....GaAlAs (λ = 780 nm)
D-A Conversion.....16 bit (Linear)
Sampling Frequency .....44.1 kHz
Conversion Rate.....88.2 kHz
Spindle Speed .....500 ~ 200 rpm (CLV)
Wow & Flutter .....Below Mesurable Limit
Frequency Response
(± 1 dB) .....5 Hz ~ 20 kHz
Total Harmonic Distortion
(1 kHz).....0.005%
Signal to Noise Ratio .....90 dB
Dynamic Range .....90 dB
Channel Separation.....85 dB
Laser Diode Properties
Material.....GaAlAs
Wavelength.....780 nm
Emission Duration .....Continuous
Laser Output Power.....Less than 44.6 μW

* This output is the value measured at a distance of 200 mm from the objective lens surface on the Optical Pick-up Block.

Audio Section

Tone Action (BASS).....100 Hz ± 8 dB
(TREBLE).....10 kHz ± 8 dB
Preout Level (Low) .....300 mV
(High).....1000 mV

General

Operating Voltage.....14.4 V (11 ~ 16 V)
Current Consumption .....0.9 A
Operating Temperature.....– 10 ~ 50 °C
Installation Size
(W × H × D) .....180 × 50 × 155 mm
(7-1/16 × 1-15/16 × 6-1/8 in.)
Weight .....1.8 kg (4.0 lb)

Kenwood follows a policy of continuous advancements in development. For this reason specifications may be changed without notice.

Kenwood poursuit une politique de progrès constants en ce qui doncerne le développement. Pour cette raison, les spécifications sont sujettes à modifications sans préavis.

Kenwood strebt ständige, Verbesserungen in der Entwicklung an. Daher bleiben Änderungen der technischen Daten jederzeit vorbehalten.

Note:

Component and circuitry are subject to modification to insure best operation under differing local conditions. This manual is based on, the U.S. (K) standard, and provides information on regional circuit modification through use of alternate schematic diagrams, and information on regional component variations through use of parts list.

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